Ver 1.2

12-Bit 1GSPS Analog to Digital Converter

Datasheet

Part Number：B12D1000RH

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Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.1	-	-	
1.1	2017.12	Chapter	Increased function description content	
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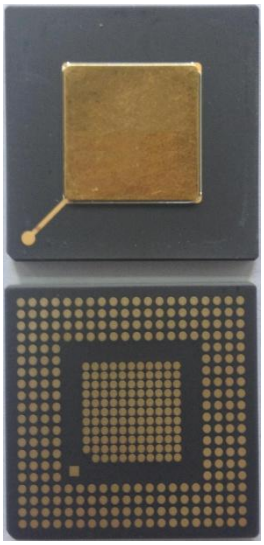
1. Features



- Configurable to Either 2.0 GSPS Interleaved or 1.0 GSPS Dual ADC
- Internally Terminated, Buffered, Differential Analog Inputs
- Interleaved Timing Automatic and Manual Skew Adjust
- Test Patterns at Output for System Debug
- 1:1 Non-demuxed or 1:2 Demuxed LVDS
- AutoSync Feature for Multi-chip Systems
- Single 1.9V ±0.1V Power Supply
- Resolution: 12 Bits
- Dual 1.0GSPS ADC, Fin = 248 MHz
  - ENOB: 9.2 Bits
  - SNR: 57.8 dB
  - SFDR: 68.2dB
  - Power: 3.2W
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV·cm^2/mg

2. Description

The B12D1000RH is a dual channel, low power, excellent performance, CMOS Analog Digital Convertor. Single 1.9V power supply, resolution 12 bits. and single channel sample select rate is 1.0 GSPS. the typical Power dissipation is 3.2 W. The chip is used the technology to assure the high quality. In order to facilitate board design and FPGA/ASIC data capture, the chip provides a flexible LVDS interface which has multiple SPI programmable. The LVDS outputs are compatible with IEEE 1596.3-1996 and support programmable common mode voltage.

The application field is focus on Wideband Communications, Data Acquisition Systems, RADAR/LIDAR, Set-top Box, Consumer RF, Software Defined Radio

3. Block Diagram

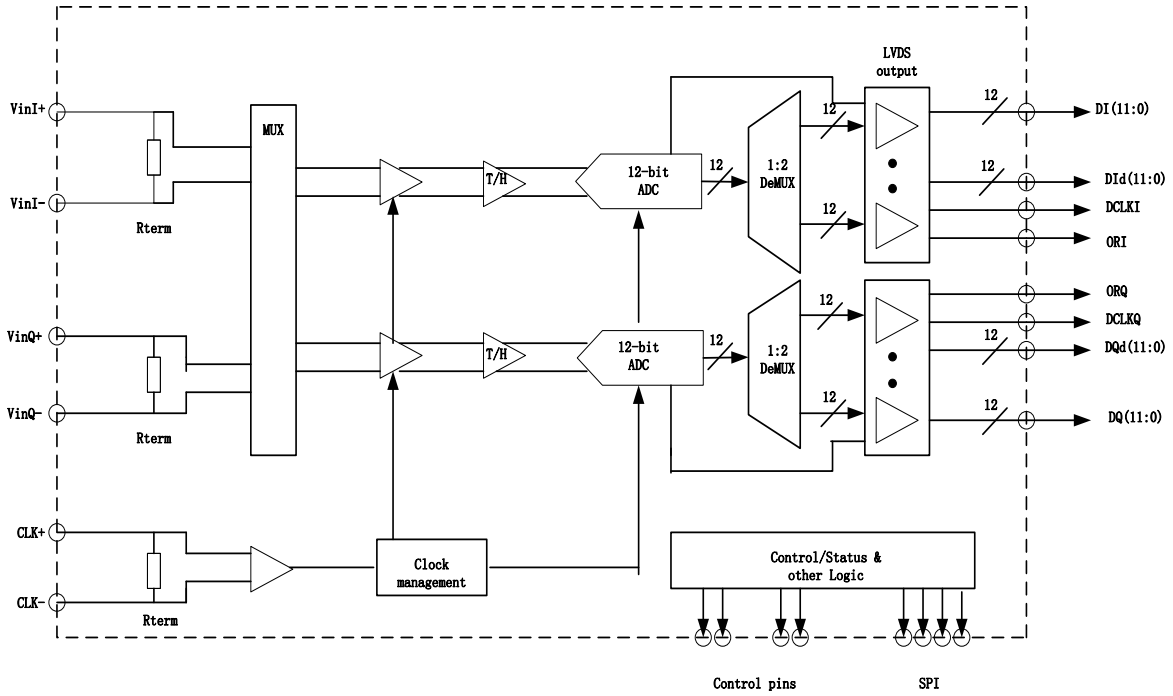


Figure 3-1. Block Diagram

4. Connection diagram

The B12D1000RH is packaged in a leaded CCGA376 package, the work temperature range is -55 ℃ to +125 ℃.

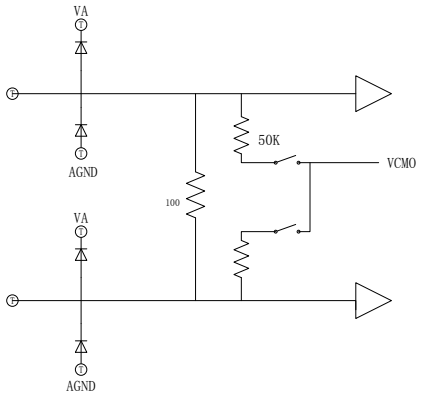
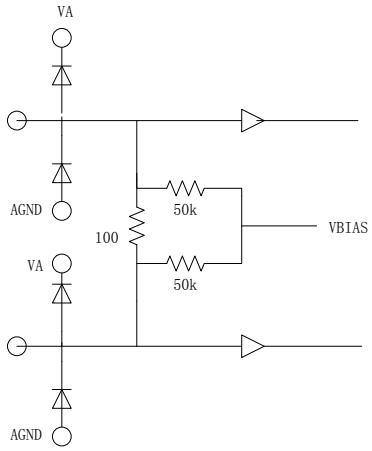
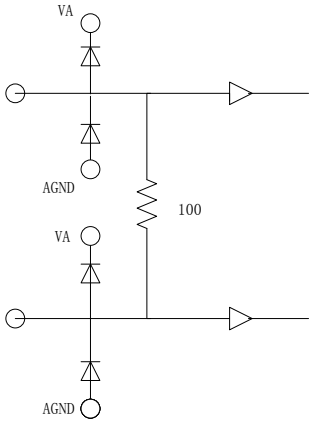
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	DId0+	V_DR	DId3+	GND_DR	DId6+	V_DR	DId9+	GND_DR	DId11+	DId11-	GND_DR	A
B	V_{BG}	GND	ECEb	SDI	CalRun	V_A	GND	GND_E	V_E	DId0-	DId2+	DId3-	DId5+	DId6-	DId8+	DId9-	DId10+	DI0+	DI1+	DI1-	B
C	Rtrim+	V_{CMO}	Rext+	SCSb	SCLK	V_A	NC	V_E	GND_E	DId1+	DId2-	DId4+	DId5-	DId7+	DId8-	DId10-	DI0-	V_DR	DI2+	DI2-	C
D	DNC	Rtrim-	Rext-	GND	GND	CAL	DNC	V_A	V_A	DId1-	V_DR	DId4-	GND_DR	DId7-	V_DR	GND_DR	V_DR	DI3+	DI4+	DI4-	D
E	V_A	Tdiode+	DNC	GND													GND_DR	DI3-	DI5+	DI5-	E
F	V_A	GND_TC	Tdiode-	DNC													GND_DR	DI6+	DI6-	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC				AA	GND	GND	GND	GND	GND	GND	GND	GND	GND	DI7+	DI7-	DI8+	DI8-	G
								AB	GND	GND	GND	GND	GND	GND	GND	GND	GND					
H	VinI+	V_TC	GND_TC	V_A				AC	GND	GND	GND	GND	GND	GND	GND	GND	GND	DI9+	DI9-	DI10+	DI10-	H
J	VinI-	GND_TC	V_TC	VbiasI				AD	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_DR	DI11+	DI11-	V_DR	J
K	GND	VbiasI	V_TC	GND_TC				AE	GND	GND	GND	GND	GND	GND	GND	GND	GND	ORI+	ORI-	DCLKI+	DCLKI-	K
L	GND	VbiasQ	V_TC	GND_TC				AF	GND	GND	GND	GND	GND	GND	GND	GND	GND	ORQ+	ORQ-	DCLKQ+	DCLKQ-	L
M	VinQ-	GND_TC	V_TC	VbiasQ				AG	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND_DR	DQ11+	DQ11-	GND_DR	M
N	VinQ+	V_TC	GND_TC	V_A				AH	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ9+	DQ9-	DQ10+	DQ10-	N
								AJ	GND	GND	GND	GND	GND	GND	GND	GND	GND					
P	V_TC	GND_TC	V_TC	V_TC				AK	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ7+	DQ7-	DQ8+	DQ8-	P
								AL	GND	GND	GND	GND	GND	GND	GND	GND	GND					
R	V_A	GND_TC	V_TC	V_TC				1	2	3	4	5	6	7	8	9	10	11	V_DR	DQ6+	DQ6-	V_DR	R
T	V_A	GND_TC	GND_TC	GND															V_DR	DQ3-	DQ5+	DQ5-	T
U	GND_TC	CLK+	PDI	GND	GND	RCOut1-	DNC	V_A	V_A	DQd1-	V_DR	DQd4-	GND_DR	DQd7-	V_DR	V_DR	GND_DR	DQ3+	DQ4+	DQ4-	U
V	CLK-	DCLK_RST+	PDQ	CalDly	DES	RCOut2+	RCOut2-	V_E	GND_E	DQd1+	DQd2-	DQd4+	DQd5-	DQd7+	DQd8-	DQd10-	DQ0-	GND_DR	DQ2+	DQ2-	V
W	DCLK_RST-	GND	DNC	DDRPh	RCLK-	V_A	GND	GND_E	V_E	DQd0-	DQd2+	DQd3-	DQd5+	DQd6-	DQd8+	DQd9-	DQd10+	DQ0+	DQ1+	DQ1-	W
Y	GND	V_A	FSR	RCLK+	RCOut1+	V_A	GND	V_E	GND_E	DQd0+	V_DR	DQd3+	GND_DR	DQd6+	V_DR	DQd9+	GND_DR	DQd11+	DQd11-	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

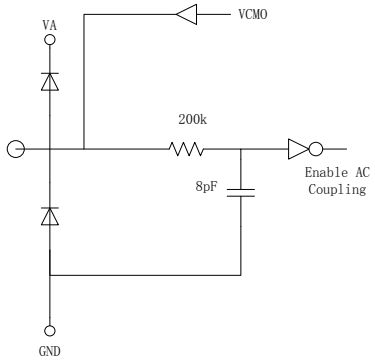
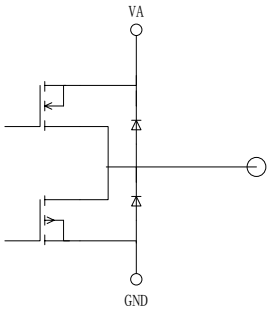
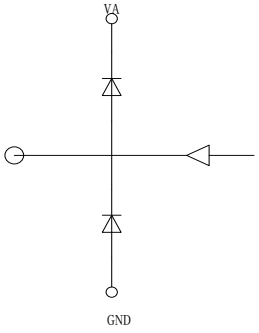
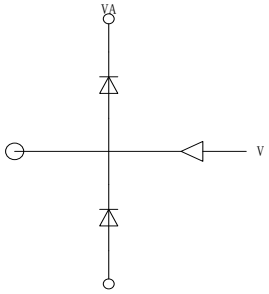
Figure 4-1. Connetion pin diagram(Top View)

The function of the pins:

Table 4-1. Analog Front-End and Clock pins

Pin No.	Name	Equivalent Circuit	Description
H1/J1 N1/M1	Vinl+/- VinQ+/-		Differential signal I-and Q-inputs. In the Non-Dual Edge Sampling (Non-DES) Mode, each I-and Q-input is sampled and converted by its respective channel. In Non-ECM (Non-Extended Control Mode) and DES Mode, both channels sample the I-input. In Extended Control Mode (ECM), the Q-input may optionally be selected for

			conversion in DES Mode by the DEQ Bit (Addr: 0h, Bit 6). Each I-and Q-channel input has an internal common mode bias that is disabled when DC-coupled Mode is selected. Both inputs must be either AC-or DC-coupled. The coupling mode is selected by the VCMO Pin. In Non-ECM, the full-scale range of these inputs is determined by the FSR Pin; both I-and Q-channels have the same full-scale input range. In ECM, the full-scale input range of the I-and Q-channel inputs may be independently set via the Control Register (Addr: 3h and Addr: Bh). Note that the high and low full-scale input range setting in Non-ECM corresponds to the mid and minimum full-scale input range in ECM. The input offset may also be adjusted in ECM.
U2/V1	CLK+/-		Differential Converter Sampling Clock. In the Non-DES Mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES Mode, the selected input is sampled on both transitions of this clock. This clock must be AC- coupled.
V2/W1	DCLK _RST+/-		Differential DCLK Reset. A positive pulse on this input is used to reset the DCLKI and DCLKQ outputs of two or more B12D1000RH in order to synchronize hem with other B12D1000RH in the system. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK input. Although supported, this feature has been superseded by AutoSync.

C2	V_{CMO}		Common Mode Voltage Output or Signal Coupling Select. If AC-coupled operation at the analog inputs is desired, this pin should be held at logic- low level. This pin is capable of sourcing/ sinking up to 100 μA. For DC-coupled operation, this pin should be left floating or terminated into high-impedance. In DC-coupled Mode, this pin provides an output voltage which is the optimal common-mode voltage for the input signal and should be used to set the common-mode voltage of the driving buffer.
B1	V_{BG}		Bandgap Voltage Output or LVDS Common- mode Voltage Select. This pin provides a buffered version of the bandgap output voltage and is capable of sourcing/sinking 100 uA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common-mode voltage. If tied to logic-high, the 1.2V LVDS common-mode voltage is selected; 0.8V is the default.
C3/D3	Rext+/-		External Reference Resistor terminals. A 3.3kΩ±0.1% resistor should be connected between Rext+/-. The Rext resistor is used as a reference to trim internal circuits which affect the linearity of the converter; the value and precision of this resistor should not be compromised.
C1/D2	Rtrim+/-		Input Termination Trim Resistor terminals. A 3.3 kΩ±0.1% resistor should be connected between Rtrim+/-. The Rtrim resistor is used to establish the calibrated 100Ωinput impedance of VinI, VinQ and CLK. These impedances may be fine tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not ensured for such an alternate value.

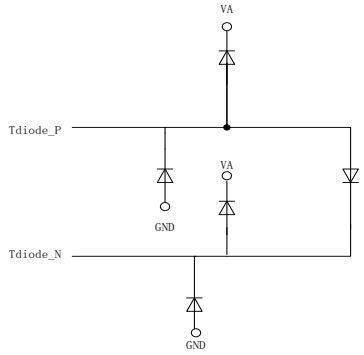
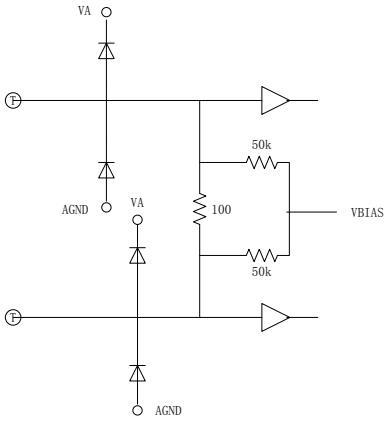
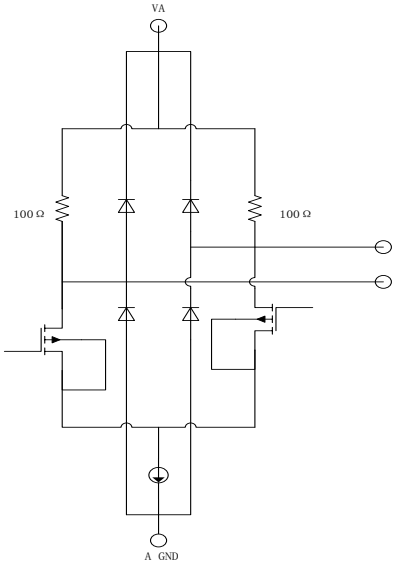
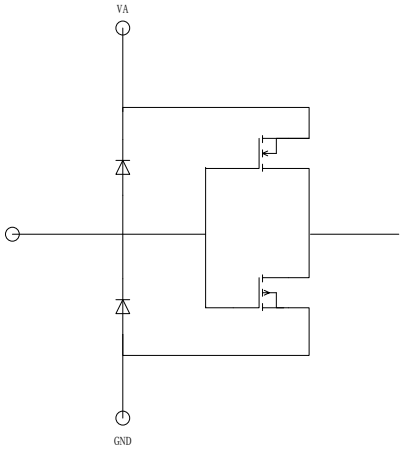
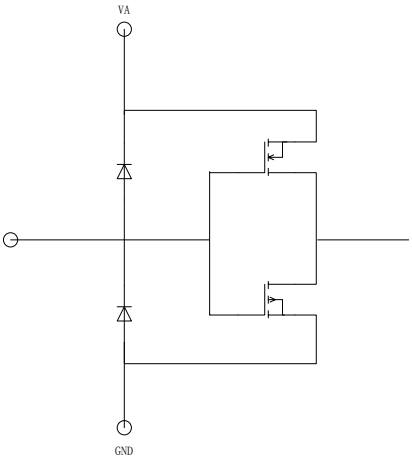
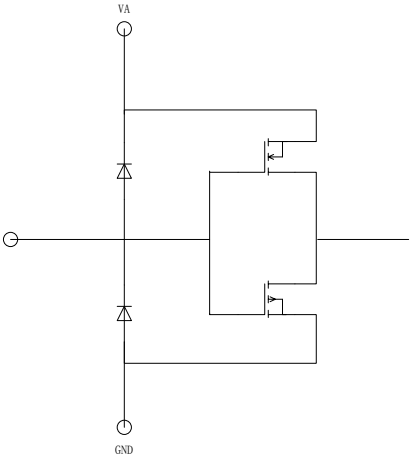
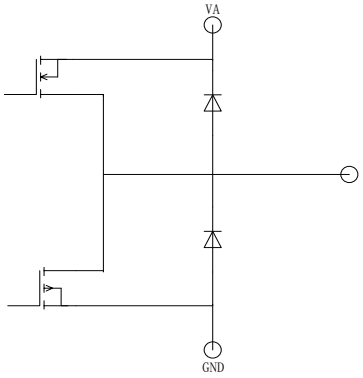
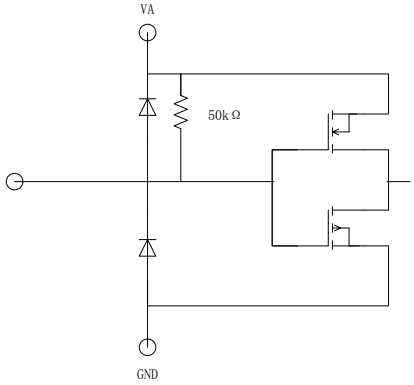
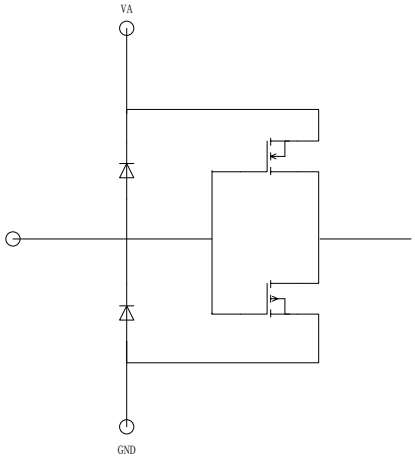
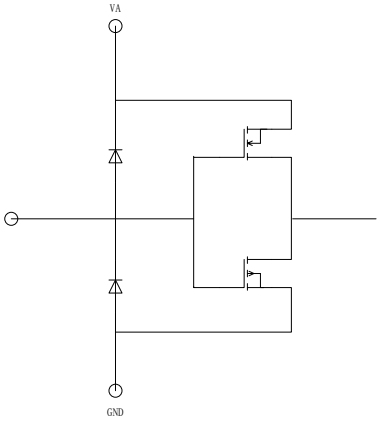
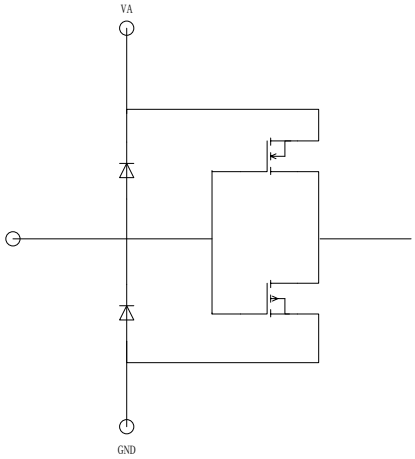
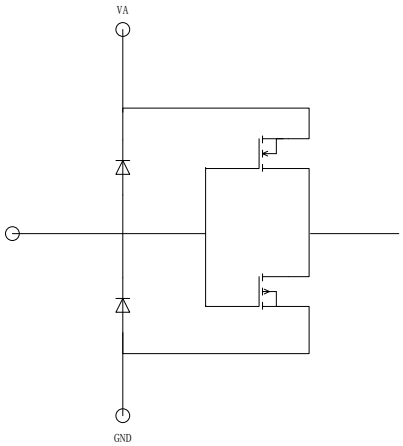
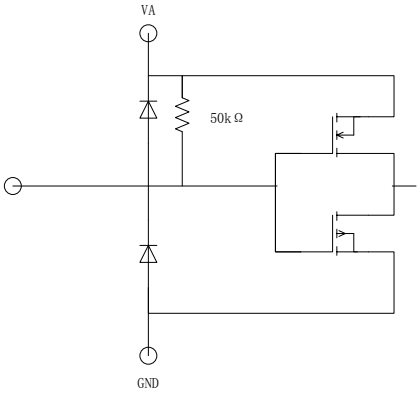
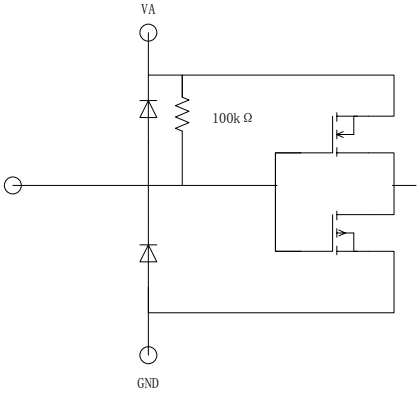
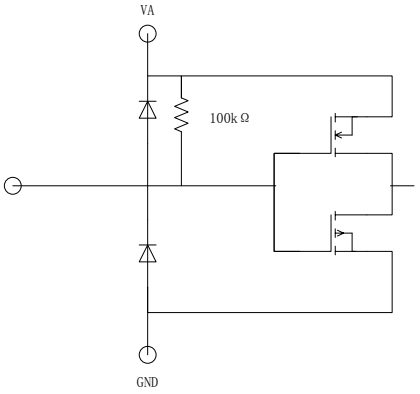
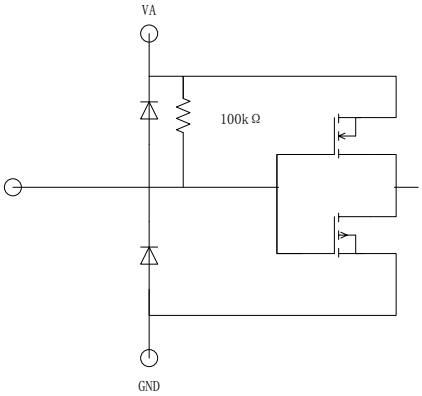
E2/F3	Tdiode+/-		Temperature Sensor Diode Positive (Anode) and Negative (Cathode) Terminals. This set of pins is used for die temperature measurements. It has not been fully characterized.
Y4/W5	RCLK+/-		Reference Clock Input. When the AutoSync feature is active, and the B12D1000RH is in Slave Mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM via Control Register (Addr: Eh).
Y5/U6 V6/V7	RCOut1+/- RCOut2+/-		Reference Clock Output 1 and 2. These signals provide a reference clock at a rate of CLK/4, when enabled, independently of whether the ADC is in Master or Slave Mode. They are used to drive the RCLK of another B12D1000RH, to enable automatic synchronization for multiple ADCs (AutoSync feature). The impedance of each trace from RCOut1 and RCOut2 to the RCLK of another B12D1000RH should be 100Ωdifferential. Having two clock outputs allows the auto-synchronization to propagate as a binary tree. Use the DOC Bit (Addr: Eh, Bit 1) to enable/ disable this feature; default is disabled.

Table 4-2. Control and Status pin

Pin No.	Name	Equivalent Circuit	Description
V5	DES		Dual Edge Sampling (DES) Mode select. In the Non-Extended Control Mode (Non-ECM), when this input is set to logic-high, the DES Mode of operation is selected, meaning that the VinI input is sampled by both channels in a time-interleaved manner. The VinQ input is ignored. When this input is set to logic-low, the device is in Non-DES Mode, i.e. the I-and Q-channels operate independently. In the Extended Control Mode (ECM), this input is ignored and DES Mode selection is controlled through the Control Register by the DES Bit (Addr: 0h, Bit 7); default is Non-DES Mode operation.
V4	CalDly		Calibration Delay select. By setting this input logic- high or logic-low, the user can select the device to wait a longer or shorter amount of time, respectively, before the automatic power-on self-calibration is initiated. This feature is pin-controlled only and is always active during ECM and Non-ECM.
D6	CAL		Calibration cycle initiate. The user can command the device to execute a self-calibration cycle by holding this input high a minimum of tCAL_H after having held it low a minimum of tCAL_L. If this input is held high at the time of power-on, the automatic power-on calibration cycle is inhibited until this input is cycled low-then-high. This pin is active in both ECM and Non-ECM. In ECM, this pin is logically OR'd with the CAL Bit (Addr: 0h, Bit 15) in the Control Register. Therefore, both pin and bit must be set low and then either can be set high to execute an on-command calibration.

B5	CalRun		Calibration Running indication. This output is logic-high while the calibration sequence is executing. This output is logic-low otherwise.
U3 V3	PDI PDQ		Power Down I-and Q-channel. Setting either input to logic-high powers down the respective I-or Q- channel. Setting either input to logic-low brings the respective I-or Q-channel to an operational state after a finite time delay. This pin is active in both ECM and Non-ECM. In ECM, each Pin is logically OR'd with its respective Bit. Therefore, either this pin or the PDI and PDQ Bit in the Control Register can be used to power-down the I-and Q-channel (Addr: 0h, Bit 11 and Bit 10), respectively.
A4	TPM		Test Pattern Mode select. With this input at logic-high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In the ECM, this input is ignored and the Test Pattern Mode can only be activated through the Control Register by the TPM Bit (Addr: 0h, Bit 12).

A5	NDM		Non-Demuxed Mode select. Setting this input to logic-high causes the digital output bus to be in the 1:1 Non-Demuxed Mode. Setting this input to logic-low causes the digital output bus to be in the 1:2 Demuxed Mode. This feature is pin-controlled only and remains active during ECM and Non-ECM.
Y3	FSR		Full-Scale input Range select. In Non-ECM, when this input is set to logic-low or logic-high, the full-scale differential input range for both I-and Q-channel inputs is set to the lower or higher FSR value, respectively. In the ECM, this input is ignored and the full-scale range of the I-and Q-channel inputs is independently determined by the setting of Addr: 3h and Addr: Bh, respectively. Note that the high (lower) FSR value in Non-ECM corresponds to the mid (min) available selection in ECM; the FSR range in ECM is greater.
W4	DDRPh		DDR Phase select. This input, when logic-low, selects the 0° Data-to-DCLK phase relationship. When logic-high, it selects the 90° Data-to-DCLK phase relationship, i.e. the DCLK transition indicates the middle of the valid data outputs. This pin only has an effect when the chip is in 1:2 Demuxed Mode, i.e. the NDM pin is set to logic-low. In ECM, this input is ignored and the DDR phase is selected through the Control Register by the DPS Bit (Addr: 0h, Bit 14); the default is 0°Mode.

B3	$\overline{\text{ECE}}$		Extended Control Enable bar. Extended feature control through the SPI interface is enabled when this signal is asserted (logic-low). In this case, most of the direct control pins have no effect. When this signal is de-asserted (logic-high), the SPI interface is disabled, all SPI registers are reset to their default values, and all available settings are controlled via the control pins.
C4	$\overline{\text{SCS}}$		Serial Chip Select bar. In ECM, when this signal is asserted (logic-low), SCLK is used to clock in serial data which is present on SDI and to source serial data on SDO. When this signal is de-asserted (logic-high), SDI is ignored and SDO is at TRI-STATE.
C5	SCLK		Serial Clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic-low, as long as timing specifications are not violated when the clock is enabled or disabled.
B4	SDI		Serial Data-In. In ECM, serial data is shifted into the device on this pin while $\overline{\text{SCS}}$ signal is asserted (logic-low).

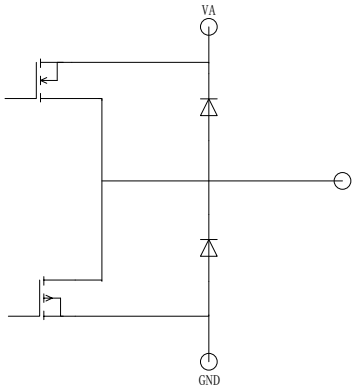
A3	SDO		Serial Data-Out. In ECM, serial data is shifted out of the device on this pin while $\overline{SCS}$ signal is asserted (logic-low). This output is at TRI-STATE when SCS is de-asserted.
D1, D7, E3, F4, W3, U7	DNC	-	Do Not Connect. These pins are used for internal purposes and should not be connected, i.e. left floating. Do not ground.
C7	NC	-	Not Connected. This pin is not bonded and may be left floating or connected to any potential.

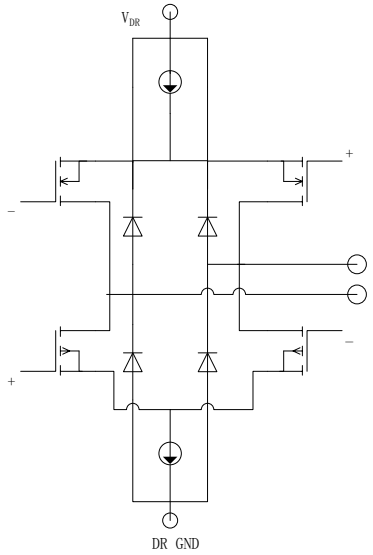
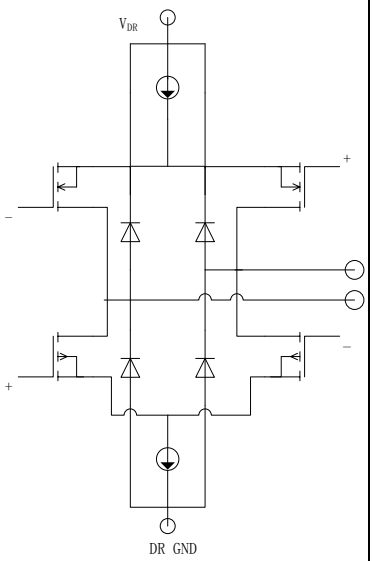
Table 4-3. Power and Ground pins

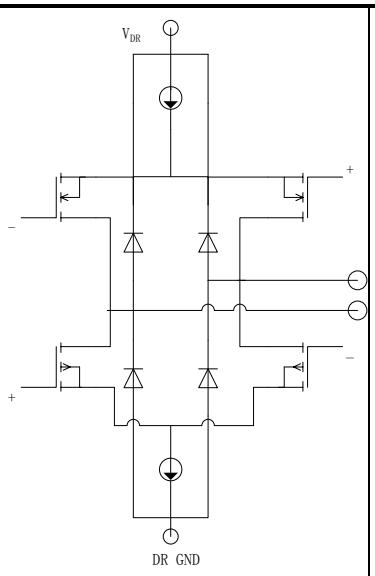
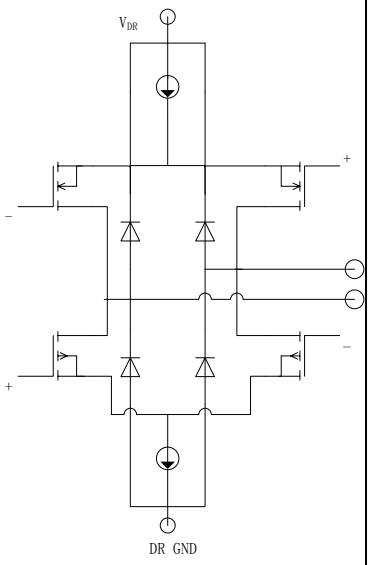
Pin No.	Name	Equivalent Circuit	Description
A2, A6, B6, C6, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A	-	Power Supply for the Analog circuitry. This supply is tied to the ESD ring. Therefore, it must be powered up before or with any other supply
G1, G3, G4, H2, J3, K3, L3, M3,N2, P1, P3, P4, R3, R4	V_{TC}	-	Power Supply for the Track-and-Hold and Clock circuitry
A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15	V_{DR}	-	Power Supply for the Output Drivers

A8, B9, C8, V8, W9, Y8	V_E	-	Power Supply for the Digital Encoder
J4, K2	V_{biasI}	-	Bias Voltage I-channel. This is an externally decoupled bias voltage for the I-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND
L2, M4	V_{biasQ}	-	Bias Voltage Q-channel. This is an externally decoupled bias voltage for the Q-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
A1, A7, B2, B7, D4, D5, E4, K1, L1, T4, U4, U5, W2, W7, Y1, Y7, AA2:AA11 AB1:AB11 AC1:AC11 AD1:AD11 AE1:AE11 AF1:AF11 AG1:AG11 AH1:AH11 AJ1:AJ11 AK1:AK11 AL1:AL11	GND	-	Ground Return for the Analog circuitry.
F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1	GND_{TC}	-	Ground Return for the Track-and-Hold and Clock circuitry
A13, A17, A20, D13, D16, E17, F17, F20, M17, M20, U13, U17,	GND_{DR}	-	Ground Return for the Output Drivers

V18, Y13, Y17, Y20			
A9, B8, C9, V9, W8, Y9	GND_E	-	Ground Return for the Digital Encoder.

Table 4-4. High-Speed Digital Outputs

Pin No.	Name	Equivalent Circuit	Description
K19/K20 L19/L20	DCLKI+/- DCLKQ+/-		Data Clock Output for the I-and Q-channel data bus. These differential clock outputs are used to latch the output data and, if used, should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver. Delayed and non-delayed data outputs are supplied synchronously to this signal. In 1:2 Demux Mode or Non-Demux Mode, this signal is at ¼ or ½ the sampling clock rate, respectively. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized
K17/K18 L17/L18	ORI+/- ORQ+/-		Out-of-Range Output for the I-and Q-channel. This differential output is asserted logic-high while the over-or under-range condition exists, i.e. the differential signal at each respective analog input exceeds the full-scale value. Each OR result refers to the current Data, with which it is clocked out. If used, each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.

J18/J19	DI11+/-		I-and Q-channel Digital Data Outputs. In Non-Demux Mode, this LVDS data is transmitted at the sampling clock rate. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data, i.e. the other ½ of the data which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. If used, each of these outputs should always be terminated with a 100Ωdifferential resistor placed as closely as possible to the differential receiver
H19/H20	DI10+/-		
H17/H18	DI9+/-		
G19/G20	DI8+/-		
G17/G18	DI7+/-		
F18/F19	DI6+/-		
E19/E20	DI5+/-		
D19/D20	DI4+/-		
D18/E18	DI3+/-		
C19/C20	DI2+/-		
B19/B20	DI1+/-		
B18/C17	DI0+/-		
M18/M19	DQ11+/-		
N19/N20	DQ10+/-		
N17/N18	DQ9+/-		
P19/P20	DQ8+/-		
P17/P18	DQ7+/-		
R18/R19	DQ6+/-		
T19/T20	DQ5+/-		
U19/U20	DQ4+/-		
U18/T18	DQ3+/-		
V19/V20	DQ2+/-		
W19/W20	DQ1+/-		
W18/V17	DQ0+/-		
A18/A19	DId11+/-		Delayed I-and Q-channel Digital Data Outputs. In Non-Demux Mode, these outputs are at TRI-STATE. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data, i.e. the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. If used, each of these outputs should always be terminated with a 100Ωdifferential resistor placed as closely as possible to the differential receiver
B17/C16	DId10+/-		
A16/B16	DId9+/-		
B15/C15	DId8+/-		
C14/D14	DId7+/-		
A14/B14	DId6+/-		
B13/C13	DId5+/-		
C12/D12	DId4+/-		
A12/B12	DId3+/-		
B11/C11	DId2+/-		
C10/D10	DId1+/-		
A10/B10	DId0+/-		
Y18/Y19	DQd11+/-		
W17/V16	DQd10+/-		
Y16/W16	DQd9+/-		
W15/V15	DQd8+/-		
V14/U14	DQd7+/-		
Y14/W14	DQd6+/-		
W13/V13	DQd5+/-		
V12/U12	DQd4+/-		

Y12/W12 W11/V11 V10/U10 Y10/W10	DQd3+/- DQd2+/- DQd1+/- DQd0+/-		

5. Electrical Characteristics

5.1 Static Characteristics

Unless otherwise specified, the following apply after calibration for V_A = V_{DR} = V_{TC} = V_E = +1.9V; I- and Q-channels, AC coupled, unused channel terminated to AC ground, FSR Pin = High; C_L = 10 pF; Differential, AC coupled Wave Sampling Clock, f_{CLK} = 1.0 GHz at 0.5 V_{P-P} with 50% duty cycle (as specified); V_{BG} = Floating; Non-Extended Control Mode; Rext = Rtrim = 3300Ω ±0.1%; Analog Signal Source Impedance = 100Ω Differential; 1:2 Demultiplex Non-DES Mode; Duty Cycle Stabilizer on. Boldface limits apply for T_A = T_{MIN} to T_{MAX}. All other limits T_A = 25 ℃.(Note 1,2,3)

Symbol	Parameter	Conditions	B12D1000RH		units
			Typ	Lim	
	Resolution with No Missing Codes			**12**	Bits
INL	Integral Non-Linearity	1 MHz DC coupled over ranged sine wave	±2.5	**±6.0**	LSB(max)
DNL	Differential Non-Linearity	1 MHz DC coupled over ranged sine wave	±0.4	**±1.0**	LSB(max)
VOFF	Offset Error		8		LSB
VOFF_ADJ	Input Offset Adjustment Range	Extended Control Mode	±40		mV
PFSE	Positive Full-Scale Error	（Note 4）		**±25**	mV(max)
NFSE	Negative Full-Scale Error	（Note 4）		**±25**	mV(max)
	Out-of-Range Output Code (Note 5)	（VIN+）-（VIN-）> + Full-Scale		**4095**	
		（VIN+）-（VIN-）< - Full-Scale		**0**	

(1) The analog inputs, are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.

(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_A = 25 ℃

(4) Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error.

(5) This parameter is specified by design and is not tested in production

5.2 Dynamic Characteristics

Symbol	Parameter	Conditions	B12D1000RH		units
			Typ	Lim	
FPBW	Full Power Bandwidth	Non-DES Mode	2.5		GHz
		DESI，DESQ Mode	1.2		GHz
		DESIQ Mode	1.7		GHz
	Gain Flatness	**Non-DES Mode**			
		D.C. to Fs/2	0.35		dB
		D.C. to Fs	0.5		dB
		DESI,DESQ Mode			
		D.C. to Fs/2	2.4		dB
		DESIQ Mode			
		D.C. to Fs/2	1.9		dB
CER	Code Error Rate		10^{-18}		Error/Sample
NPR	Noise Power Ratio		48.5		dB
Non-DES Mode(Note 1,2)					
ENOB	Effective Number of Bits	AIN=100 MHz@-0.5dBFS	9.2		bits
		AIN=248 MHz @-0.5 dBFS	9.2	**8.3**	bits(min)
		AIN=498 MHz @-0.5 dBFS	9.0		bits(min)
		AIN=998 MHz @-0.5 dBFS	8.7		bits
SINAD	Signal-to-Noise Plus Distortion Ratio	AIN=100 MHz @-0.5 dBFS	57.2		dB
		AIN=248 MHz @-0.5 dBFS	56.5	**51.8**	dB(min)
		AIN=498 MHz @-0.5 dBFS	56.1		dB(min)
		AIN=998 MHz @-0.5 dBFS	54.1		dB
SNR	Signal-to-Noise Ratio	AIN= 100 MHz @-0.5 dBFS	58.2		dB
		AIN= 248 MHz @-0.5 dBFS	57.3	**52.3**	dB(min)
		AIN= 498 MHz @-0.5 dBFS	56.5		dB(min)
		AIN= 998 MHz @-0.5 dBFS	54.5		dB
THD	Total Harmonic Distortion	AIN= 100 MHz @-0.5 dBFS	-64.0		dB
		AIN= 248 MHz @-0.5 dBFS	-63.4	**-56.5**	dB(max)
		AIN= 498 MHz @-0.5 dBFS	-62.9		dB(max)
		AIN= 998 MHz @-0.5 dBFS	-59.2		dB
SFDR	Spurious-Free	AIN= 100 MHz @-0.5 dBFS	61.2		dB

	Dynamic Range	AIN= 248 MHz @-0.5 dBFS	60.6	**57**	dB(min)
		AIN= 498 MHz @-0.5 dBFS	60.4		dB(min)
		AIN= 998 MHz @-0.5 dBFS	59.9		dB
DES Mode(Note 1,2,3)					
ENOB	Effective Number of Bits	AIN= 100 MHz @-0.5 dBFS	9.2		bits
		AIN= 248 MHz @-0.5 dBFS	9.1		bits(min)
		AIN= 498 MHz @-0.5 dBFS	8.9		bits
		AIN= 998 MHz @-0.5 dBFS	8.6		bits
SINAD	Signal-to-Noise Plus Distortion Ratio	AIN= 100 MHz @-0.5 dBFS	57.2		dB
		AIN= 248 MHz @-0.5 dBFS	56.5		dB(min)
		AIN= 498 MHz @-0.5 dBFS	56.1		dB
		AIN= 998 MHz @-0.5 dBFS	53.5		dB
SNR	Signal-to-Noise Ratio	AIN= 100 MHz @-0.5 dBFS	57.6		dB
		AIN= 248 MHz @-0.5 dBFS	57.1		dB(min)
		AIN= 498 MHz @-0.5 dBFS	56.6		dB
		AIN= 998 MHz @-0.5 dBFS	54.1		dB
THD	Total Harmonic Distortion	AIN= 100 MHz @-0.5 dBFS	-61.8		dB
		AIN= 248 MHz @-0.5 dBFS	-60.1		dB(max)
		AIN= 498 MHz @-0.5 dBFS	-59.0		dB
		AIN= 998 MHz @-0.5 dBFS	-58.0		dB
SFDR	Spurious-Free Dynamic Range	AIN= 100 MHz @-0.5 dBFS	62.4		dB
		AIN= 248 MHz @-0.5 dBFS	59.0		dB(min)
		AIN= 498 MHz @-0.5 dBFS	58.2		dB
		AIN= 998 MHz @-0.5 dBFS	53.7		dB

(1) The Dynamic Specifications are ensured for room to hot ambient temperature only (25 ℃ to 125 ℃).

(2) The Fs/2 spur was removed from all the dynamic performance specifications.

(3) These measurements were taken in Extended Control Mode (ECM) with the DES Timing Adjust feature enabled (Addr: 7h). This feature is used to reduce the interleaving timing spur amplitude, which occurs at fs/2-fin, and thereby increase the SFDR, SINAD and ENOB.

5.3 Analog Input/Output and Reference Characteristics

Symbol	Parameter	Conditions	B12D1000RH		Unit
			typ	lim	
Analog Inputs					
V_{IN_FSR}	Analog Differential Input Full Scale Range	FSR Pin Low	600	**540**	mV_{P-P}(min)
				660	mV_{P-P}(max)
		FSR Pin High	800	**740**	mV_{P-P}(min)
				860	mV_{P-P}(max)
		Extended Control Mode			

		FM（14：0）= 0000h	600		mV_{P-P}
		FM（14：0）= 4000h (Default)	800		mV_{P-P}
		FM（14：0）= 7FFFh	1000		mV_{P-P}
C_{IN}	Analog Input Cap-acitanc	Differential	4.2		pF
		Each input pin to ground	17.2		pF
R_{IN}	Differential Input Resistance		100	**91**	Ω(min)
				109	Ω(max)
Common Mode Output					
V_{CMO}	Common Mode Output Voltage	Icmo = ±100μA	1.25	**1.15**	V(min)
				1.35	V(max)
TC_V_{CMO}	Common Mode Output Voltage Temperature Coefficient	Icmo = ±100μA	180		ppm/℃
V_{CMO_LVL}	V_{CMO} input threshold to set DC-coupling Mode		0.63		V
$C_{L\_}V_{CMO}$	Maximum V_{CMO} Load Capacitance	(Note 1)		**80**	pF
Bandgap Reference					
V_{BG}	Bandgap Reference Output Voltage	I_{BG}= ±100μA	1.25	**1.15**	V(min)
				1.35	V(max)
TC_V_{BG}	Bandgap Reference Voltage Temperature Coefficient	I_{BG}= ±100μA	160		ppm/℃
$C_{L\_}V_{BG}$	Maximum Bandgap Reference load Capacitance	（Note 1）		**80**	pF

(1) This parameter is specified by design and is not tested in production

5.4 I-Channel to Q-Channel Characteristics

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
	Offset Match		5		LSB
	Positive Full-Scale Match	Zero offset selected in Control Register	5		LSB
	Negative Full-Scale Match	Zero offset selected in Control Register	5		LSB
	Phase Matching（I,Q）	f_{IN} = 1.0 GHz	< 2		Degree

5.5 Sampling Clock Characteristics

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
V_{IN_CLK}	Differential Sampling Clock Input Level （Note 1）	Sine Wave Clock Differential Peak-to-Peak	0.6	**0.4**	V_{P-P}(min)
				2.0	V_{P-P}(max)
		Square Wave Clock Differential Peak-to-Peak	0.6	**0.4**	V_{P-P}(min)
				2.0	V_{P-P}(max)
C_{IN_CLK}	Sampling Clock Input Capacitance （Note 1）	Differential	4.4		pF
		Each input to ground	17.5		pF
R_{IN_CLK}	Sampling Clock Differential Input Resistance		100		Ω

（1）This parameter is specified by design and is not tested in production

5.6 AutoSync Feature Characteristics

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
V_{IN_RCLK}	Differential RCLK Input Level	Differential Peak-to-Peak	360		mV_{P-P}
C_{IN_RCLK}	RCLK Input Capacitance	Differential	4.4		pF
		Each input to ground	17.5		pF
R_{IN_RCLK}	RCLK Differential Input Resistance		100		Ω
I_{IH_RCLK}	Input Leakage Current; $V_{IN}=V_A$		22		μA
I_{IL_RCLK}	Input Leakage Current，V_{IN}=GND		-33		μA
V_{O_RCOUT}	Differential RCOut Output Voltage		600		mV

5.7 Digital Control and Output Pin Characteristics

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
Digital Control Pins （DES,CalDly,CAL,PDI,PDQ,TPM,NDM,FSR,DDRPh,$\overline{ECE}$,SCLK,SDI,$\overline{SCS}$）					
V_{IH}	Logic High Input Voltage			**0.7×V_A**	V(min)
V_{IL}	Logic Low Input			**0.3×V_A**	V(max)

	Voltage				
I_{IH}	Input Leakage Current，$V_{IN} = V_A$		0.02		μA
I_{IL}	Input Leakage Current，V_{IN} = GND	FSR,CalDly,CAL, NDM,TPM,DDRPh,DES	-0.02		μA
		$\overline{SCS}$,SCLK,$\overline{SDI}$ PDI,PDQ,$\overline{ECE}$	-38		μA
C_{IN_DIG}	Digital Control Pin Input Capacitance (Note 1)		4		pF
Digital Output Pins（Data,DCLKI,DCLKQ,ORI,ORQ）					
V_{OD}	LVDS Differential Output Voltage	V_{BG}= Floating，OVS= High	630	**400**	mV_{P-P}(min)
				800	mV_{P-P}(max)
		V_{BG}= Floating，OVS= Low	460	**230**	mV_{P-P}(min)
				630	mV_{P-P}(max)
		$V_{BG} = V_A$，OVS= High	670		mV_{P-P}
		$V_{BG} = V_A$，OVS= Low	500		mV_{P-P}
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels		±5		mV
V_{OS}	Output Offset Voltage	V_{BG}= Floating	0.8		V
		$V_{BG} = V_A$	1.2		V
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±5		mV
I_{OS}	Output Short Circuit Current	V_{BG}= Floating，D+ and D−connected to 0.8V	±4		mA
Z_O	Differential Output Impedance	100	100		Ω
V_{OH}	Logic High Output Level		1.65		V
V_{OL}	Logic Low Output Level		0.15		V
Differential DCLK Reset Pins（DCLK_RST）					
V_{CMI_DRST}	DCLK_RST Common Mode Input Voltage		1.25		V

V_{ID_DRST}	Differential DCLK_RST Input Voltage		V_{IN_CLK}		V_{P-P}
R_{IN_DRST}	Differential DCLK_RST Input Resistance		100		Ω

（1）This parameter is specified by design and is not tested in production

5.8 Power Supply Characteristics

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
I_A	Analog Supply Current	PDI 、 PDQ = Low	960	**1195**	mA
		PDI =Low； PDQ = High	520		mA
		PDI = High； PDQ =Low	520		mA
		PDI 、PDQ = High	15		mA
I_{TC}	Track-and-Hold and Clock Supply current	PDI 、 PDQ=Low	350	**430**	mA
		PDI =Low； PDQ = High	220		mA
		PDI = High； PDQ =Low	220		mA
		PDI 、PDQ = High	4		mA
I_{DR}	Output Driver Supply Current	PDI 、 PDQ =Low	270	**340**	mA
		PDI =Low； PDQ = High	140		mA
		PDI = High； PDQ =Low	140		mA
		PDI 、PDQ = High	3		mA
I_E	Digital Encoder Supply Current	PDI 、 PDQ =Low	100	**140**	mA
		PDI =Low； PDQ = High	50		mA
		PDI = High； PDQ =Low	50		mA
		PDI 、PDQ = High	1		mA
I_{TOTAL}	Total Supply Current	1:2 DemuxMode PDI 、 PDQ =Low	1680	**2105**	mA
		Non DemuxMode PDI 、 PDQ =Low	1570		mA
Pc	Power Consumption	1:2 DemuxMode			
		PDI 、 PDQ =Low	3.2	**4.0**	W(max)
		PDI =Low； PDQ = High	1.75		W
		PDI = High； PDQ =Low	1.75		W
		PDI 、PDQ = High	43		mW
		Non DemuxMode			
		PDI 、 PDQ =Low	2.98		W(max)

5.9 AC Electrical Characteristics

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
Sampling Clock (CLK)					

$f_{CLK(max)}$	Maximum Sampling Clock Frequency			**1.0**	GHz
$f_{CLK(min)}$	Minimum Sampling Clock Frequency	Non DES Mode；LFS = 0b		**300**	MHz
		Non DES Mode；LFS = 1b		**150**	MHz
		DESMode		**500**	MHz
	Sampling Clock Duty Cycle	$f_{CLK(min)} \leq f_{CLK} \leq f_{CLK(max)}$	50	**20**	%(min)
				80	%(max)
t_{CL}	Sampling Clock Low Time		500	**200**	ps(min)
t_{CH}	Sampling Clock High Time		500	**200**	ps(max)
Data Clock (DCLKI,DCLKQ)					
	DCLK Duty Cycle	（Note 1）	50	**45**	%(min)
				55	%(max)
t_{SR}	DCLK_RST±Setup Time	（Note 1）	45		ps
t_{HR}	DCLK_RST±Hold Time	（Note 1）	45		ps
t_{PWR}	DCLK_RST±Pulse Width	（Note 1）		**5**	Sampling Clock Cycles (min)
t_{SYNV_DLY}	DCLK Synchronization Delay	90 °Mode （Note 1）		**4**	Sampling Clock Cycles (min)
		0 °Mode （Note 1）		**5**	
t_{LHT}	Differential Low-to-High Transition Time	10%~90% ，C_L=2.5pF	200		ps
t_{HLT}	Differential High-to-Low Transition Time	10%~90% ，C_L=2.5pF	200		ps
t_{SU}	Data-to-DCLK Setup Time	90 °Mode （Note 1）	780		ps
t_H	DCLK-to-Data Hold Time	90 °Mode （Note 1）	780		ps
t_{OSK}	DCLK-to-Data Output Skew	50% of DCLK transition to 50% of Data transition （Note 1）	±50		ps(max)

Data Input-to-Output					
t_{AD}	Aperture Delay	Sampling CLK+ Rise to Acquisition of Data	1.15		ns
t_{AJ}	Aperture Jitter		0.2		ps(rms)
t_{OD}	Sampling Clock-to Data Output Delay	50% of Sampling Clock transition to 50% of Data transition	3.2		ns
t_{LAT}	Latency in 1:2 Demux Non-DES Mode	DI,DQOutput		**34**	Sampling Clock Cycles
		DId,DQdOutput		**35**	
	Latency in 1:4 Demux Non-DES Mode	DIOutput		**34**	
		DQOutput		**34.5**	
		DIdOutput		**35**	
		DQdOutput		**35.5**	
	Latency in Non-Demux Non-DES Mode	DIOutput		**34**	
		DQOutput		**34**	
	Latency in Non-Demux DES Mode	DIOutput		**34**	
		DQOutput		**34.5**	
t_{ORR}	Over Range Recovery Time		1		Sampling Clock Cycles
t_{WU}	Wake-Up Time (PDI/ PDQ low to Rated Accuracy Conversion)		4		us

（1）This parameter is specified by design and is not tested in production

5.10 Serial Port Interface

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
f_{SCLK}	Serial Clock Frequency	（Note 1）	15		MHz
	Serial Clock Low Time			**30**	ns(min)
	Serial Clock High Time			**30**	ns(min)
t_{SSU}	Serial Data-to-Serial	（Note 1）	3		ns(min)

	Clock Rising Setup Time				
t_{SH}	Serial Data-to-Serial Clock Rising Hold Time	（Note 1）	1.5		ns(min)
t_{SCS}	$\overline{SCS}$-to-Serial Clock Rising Setup Time		3		ns
t_{HCS}	$\overline{SCS}$-to-Serial Clock Falling Hold Time		2		ns
t_{BSU}	Bus turn-around time		15		ns

（1）This parameter is specified by design and is not tested in production

5.11 Calibration

Symbol	Parameter	Conditions	B12D1000RH		units
			typ	lim	
t_{CAL}	Calibration Cycle Time	CSS = 0b	5.2×10^7		Sampling Clock Cycles
		CSS = 1b			
t_{CAL_L}	CAL Pin Low Time	（1）		**1280**	Sampling Clock Cycles (min)
t_{CAL_H}	CAL Pin High Time	（1）		**1280**	
t_{CalDly}	Calibration delay determined by CalDly	CalDly=Low		$\mathbf{2^{24}}$	Sampling Clock Cycles (max)
		CalDly= High		$\mathbf{2^{30}}$	

（1）This parameter is specified by design and is not tested in production

6. Absolute Maximum Ratings(Note 1,2)

Supply Voltage（V_A，V_{TC}，V_{DR}，V_E）	2.2V
Supply Difference max($V_{A/TC/DR/E}$) – min ($V_{A/TC/DR/E}$)	0V ~ 100mV
Voltage on Any Input Pin（Except $V_{IN+/-}$）	-0.15V ~（V_A+0.15V）
V_{IN}+/- Voltage Range	-0.5V ~ 2.5V
Ground Difference max($GND_{TC/DR/E}$)-min($GND_{TC/DR/E}$)	0V ~ 100mV
Input Current at Any Pin (Note 3)	±50mA
Power Dissipation T_A <= 125℃	3.8W
ESD Susceptibility (Human Body Model)	2000V
Storage Temperature	-65℃ ~ +150℃

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance

limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) All voltages are measured with respect to GND = GND_{TC} = GND_{DR} = GND_E = 0V, unless otherwise specified.

(3) When the input voltage at any pin exceeds the power supply limits, i.e. less than GND or greater than V_A, the current at that pin should be limited to 50 mA. In addition, over-voltage at a pin must adhere to the maximum voltage limits. Simultaneous over-voltage at multiple pins requires adherence to the maximum package power dissipation limits.

7. Operating Ratings(Note 1,2)

Ambient Temperature Range	-55℃≤ T_A ≤+125℃
Junction Temperature Range(applies only to maximum operating speed)	T_j ≤ +140℃
Supply Voltage(V_A， V_{TC}， V_E)	+1.8V ~ +2.0V
Driver Supply Voltage(V_{DR})	+1.8V ~ V_A
V_{IN}+/- Voltage Range(Note 3)	0.4V ~ 2.4V（d.c.-coupled）
V_{IN}+/- Current Range(Note 3)	±50mA (a.c.-coupled)
V_{IN}+/- Power	15.3dBm（(maintaining common mode voltage, a.c.-coupled）
Ground Differencemax($GND_{TC/DR/E}$)-min($GND_{TC/DR/E}$)	0V
CLK+/- Voltage Range	0V ~ V_A
Differential CLK Amplitude	0.4Vp-p ~ 2.0Vp-p
Common Mode Input Voltage	V_{CMO}–150mV < V_{CMI} < V_{CMO}+150mV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) All voltages are measured with respect to GND = GND_{TC} = GND_{DR} = GND_E = 0V, unless otherwise specified.

(3) Proper common mode voltage must be maintained to ensure proper output codes, especially during input overdrive.

8. Transfer Characteristic and Timing Diagrams

8.1 Transfer Characteristic

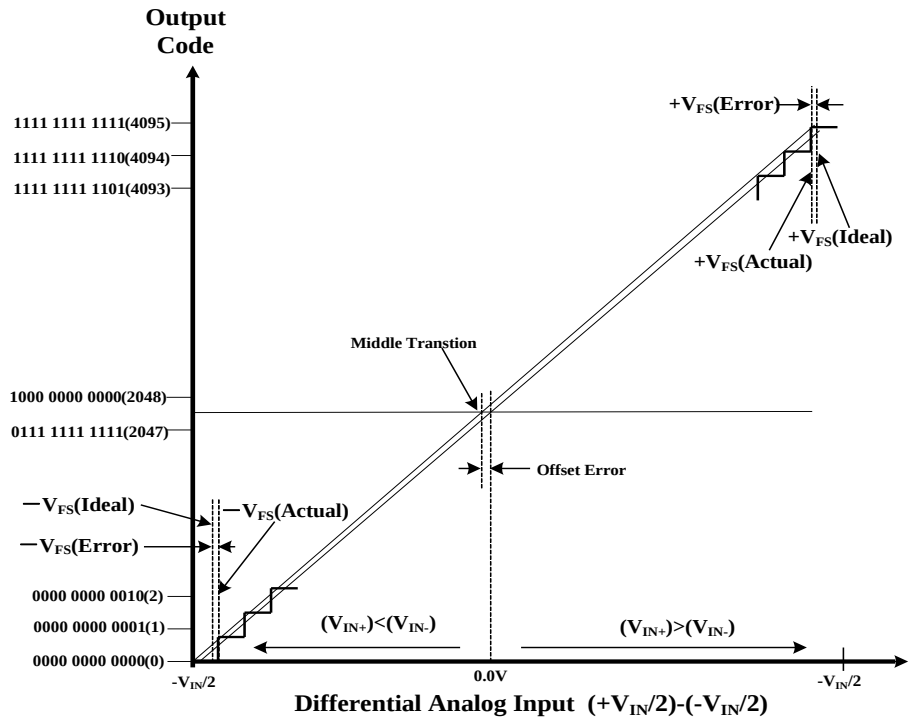


Figure 8-1. Input / Output Transfer Characteristic

8.2 Timing Diagrams

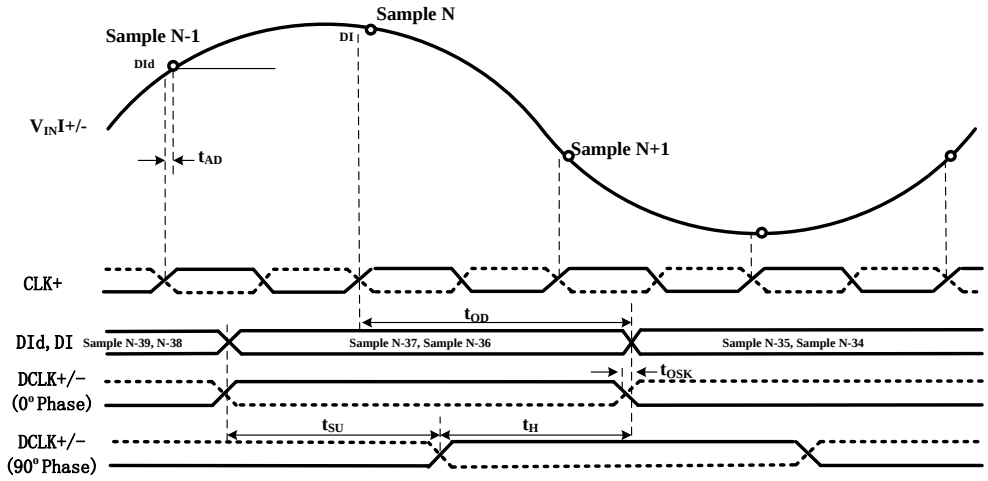


Figure 8-2. Clock in 1:2 Demux Non-DES Mode

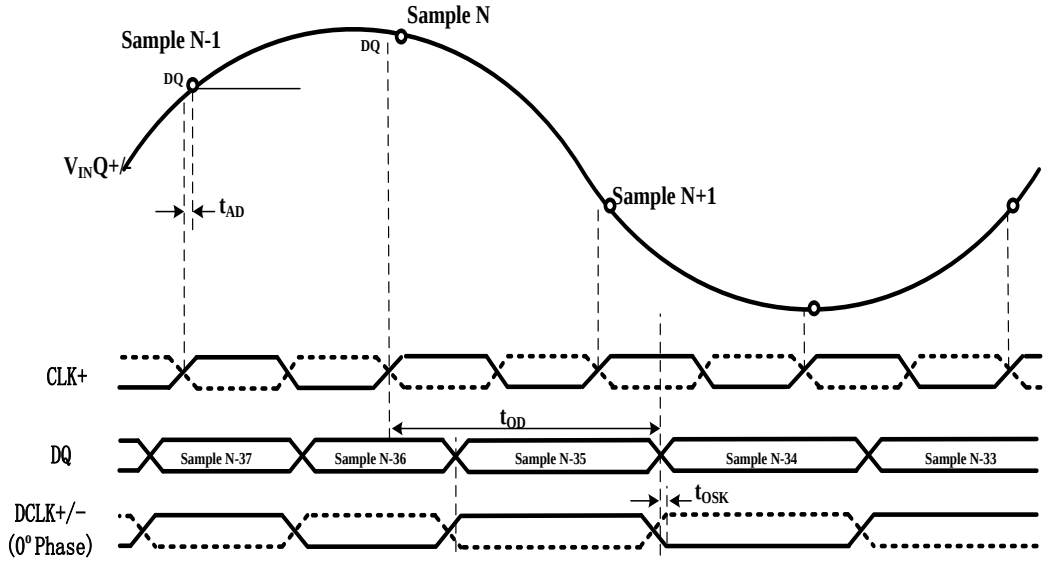


Figure 8-3. Clocking in Non-Demux Non-DES Mode

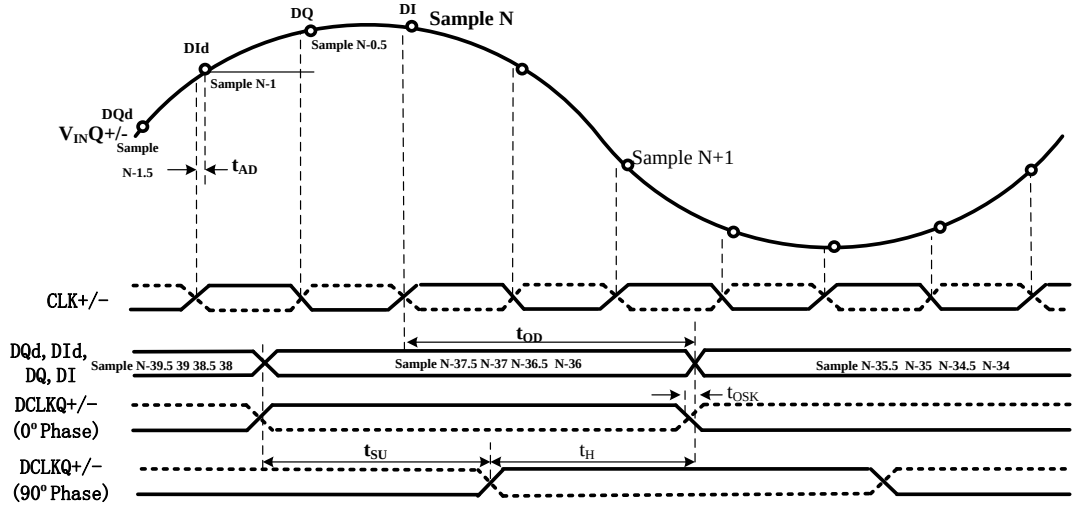


Figure 8-4. Clocking in 1:4 Demux DES Mode

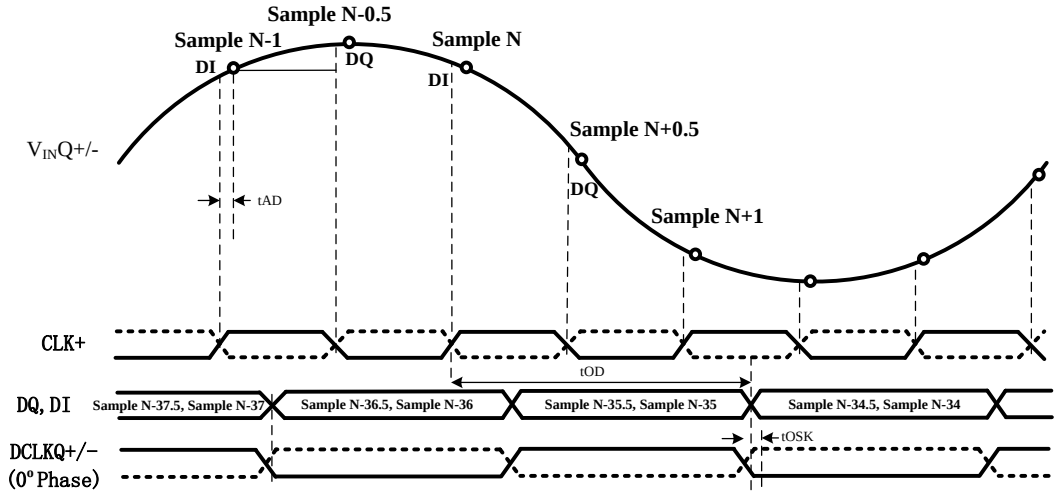


Figure 8-5. Clocking in Non-Demux Mode DES Mode

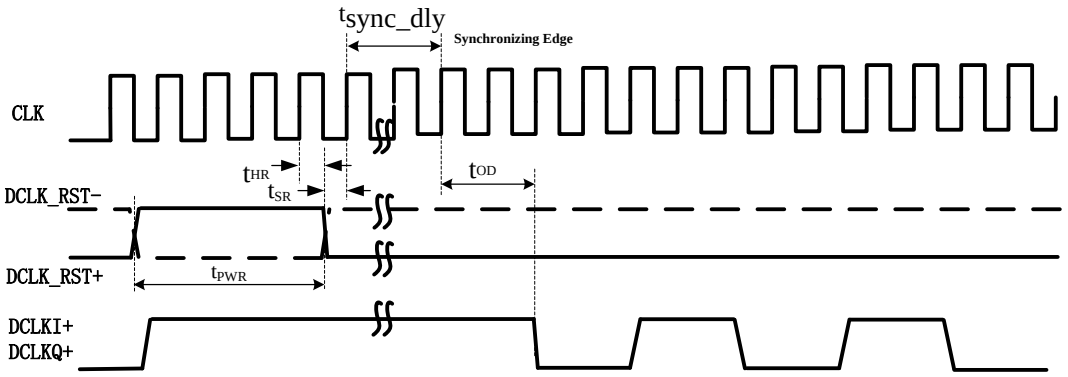


Figure 8-6. Data Clock Reset Timing（Demux Mode）

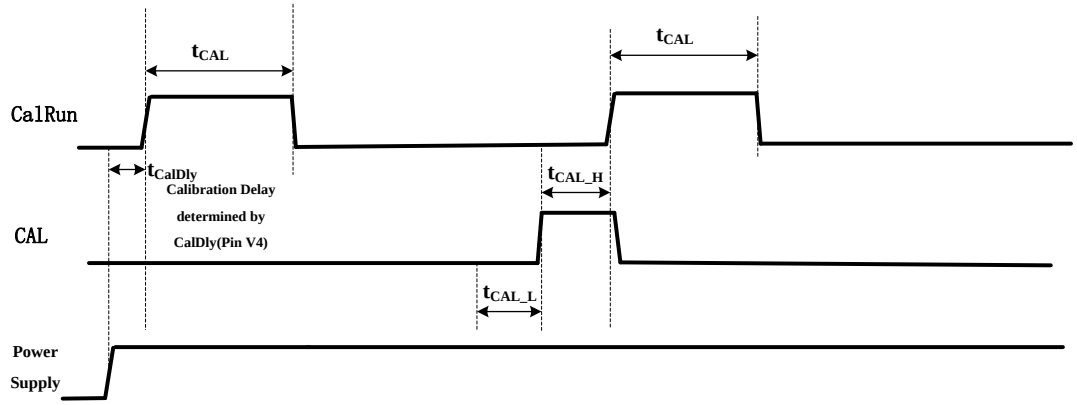


Figure 8-7. Power-on and On-Command Calibration Timing

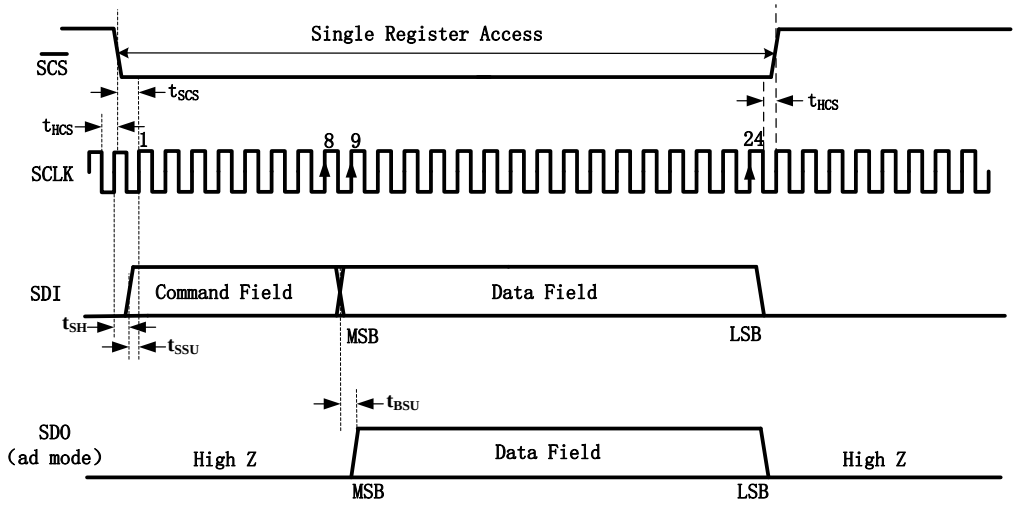


Figure 8-8. Serial Interface Timing

9. Function Description

The B12D1000RH is a versatile A/D converter with an innovative architecture which permits very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section. This section

covers an overview, a description of control modes (Extended Control Mode and Non-Extended Control Mode), and features.

9.1 Overview

The B12D1000RH uses a calibrated folding and interpolating architecture that achieves a high Effective Number of Bits (ENOB). The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to correcting other non-idealities, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal (which is within the converter's input voltage range) is digitized to twelve bits at speeds of 150 MSPS to 2.0 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the I- or Q-input will cause the Out-of-Range I-channel or Qchannel output (ORI or ORQ), respectively, to output a logic-high signal.

Each channel has a selectable output demultiplexer which feeds two LVDS buses. If the 1:2 Demux Mode is selected, the output data rate is reduced to half the input sample rate on each bus. When Non-Demux Mode is selected, the output data rate on each channel is at the same rate as the input sample clock and only one 12-bit bus per channel is active.

9.2 Control Modes

The B12D1000RH may be operated in one of two control modes: Non-extended Control Mode (Non-ECM) or Extended Control Mode (ECM). In the simpler Non-ECM (also sometimes referred to as Pin Control Mode), the user affects available configuration and control of the device through the control pins. The ECM provides additional configuration and control options through a serial interface and a set of 16 registers, most of which are available to the customer.

Non-Extended Control Mode

In Non-extended Control Mode (Non-ECM), the Serial Interface is not active and all available functions are controlled via various pin settings. Non-ECM is selected by setting the ECE Pin to logic-high. Note that, for the control pins, "logic-high" and "logic-low" refer to V_A and GND, respectively. Nine dedicated control pins provide a

wide range of control for the B12D1000RH and facilitate its operation. These control pins provide DES Mode selection, Demux Mode selection, DDR Phase selection, execute Calibration, Calibration Delay setting, Power Down I-channel, Power Down Q-channel, Test Pattern Mode selection, and Full-Scale Input Range selection. In addition to this, two dual-purpose control pins provide for AC/DC-coupled Mode selection and LVDS output common-mode voltage selection. See Table 9-1 for a summary.

Table 9-1 Non-ECM Pin Summary

Pin Name	Logic Low	Logic High	Floating
Dedicated Control Pins			
DES	Non-DES Mode	DES Mode	Not valid
NDM	Demux Mode	Non- Demux Mode	Not valid
DDRPh	0 °Mode	90 °Mode	Not valid
CAL	See Calibration Pin（*CAL*）		Not valid
CalDly	Shorter delay	Longer delay	Not valid
PDI	I-channel active	Power Down I-channel	Power Down I-channel
PDQ	Q-channel active	Power Down Q-channel	Power Down Q-channel
TPM	Non-Test Pattern Mode	Test Pattern Mode	Not valid
FSR	Lower FS input Range	Higher FS input Range	Not valid
Dual-purpose Control Pins			
V_{CMO}	AC-coupled operation	Not allowed	DC-coupled operation
V_{BG}	Not allowed	Higher LVDS common-mode voltage	Lower LVDS common-mode voltage

Dual Edge Sampling Pin (DES)

The Dual Edge Sampling (DES) Pin selects whether the B12D1000RH is in DES Mode (logic-high) or Non-DES Mode (logic-low). DES Mode means that a single analog input is sampled by both I- and Q-channels in a time-interleaved manner. One of the ADCs samples the input signal on the rising sampling clock edge (duty cycle corrected); the other ADC samples the input signal on the falling sampling clock edge (duty cycle corrected). In Non-ECM, only the I-input may be used for DES Mode, a.k.a. DESI Mode. In ECM, the Q-input may be selected via the DEQ Bit (Addr: 0h, Bit: 6), a.k.a. DESQ Mode. In ECM, both the I- and Q-inputs may be selected, a.k.a. DESIQ Mode.

To use this feature in ECM, use the DES bit in the Configuration Register (Addr: 0h; Bit: 7). See DES/Non-DES Mode for more information.

Non-Demultiplexed Mode Pin (NDM)

The Non-Demultiplexed Mode (NDM) Pin selects whether the B12D1000RH is in Demux Mode (logic-low) or Non-Demux Mode (logic-high). In Non-Demux Mode,

the data from the input is produced at the sampled rate at a single 12-bit output bus. In Demux Mode, the data from the input is produced at half the sampled rate at twice the number of output buses. For Non-DES Mode, each I- or Q-channel will produce its data on one or two buses for Non-Demux or Demux Mode, respectively. For DES Mode, the selected channel will produce its data on two or four buses for Non-Demux or Demux Mode, respectively.

This feature is pin-controlled only and remains active during both Non-ECM and ECM. See Demux/Non-demux Mode for more information.

Dual Data Rate Phase Pin (DDRPh)

The Dual Data Rate Phase (DDRPh) Pin selects whether the B12D1000RH is in 0 ° Mode (logic-low) or 90 ° Mode (logic-high). The Data is always produced in DDR Mode on the B12D1000RH. The Data may transition either with the DCLK transition (0 °Mode) or halfway between DCLK transitions (90 °Mode). The DDRPh Pin selects 0 ° Mode or 90 ° Mode for both the I-channel: DI and DId-to-DCLKI phase relationship and for the Q-channel: DQ and DQd-to-DCLKQ phase relationship.

To use this feature in ECM, use the DPS bit in the Configuration Register (Addr: 0h; Bit: 14). See DDR Clock Phase for more information.

Calibration Pin (CAL)

The Calibration (CAL) Pin may be used to execute an on-command calibration or to disable the power-on calibration. The effect of calibration is to maximize the dynamic performance. To initiate an on-command calibration via the CAL pin, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles. Holding the CAL pin high upon power-on will prevent execution of the power-on calibration. In ECM, this pin remains active and is logically OR'd with the CAL bit.

To use this feature in ECM, use the CAL bit in the Configuration Register (Addr: 0h; Bit: 15). See Calibration Feature for more information.

Calibration Delay Pin (CalDly)

The Calibration Delay (CalDly) Pin selects whether a shorter or longer delay time is present, after the application of power, until the start of the power-on calibration. The actual delay time is specified as t_{CalDly} and may be found in Calibration. This feature is pin-controlled only and remains active in ECM. It is recommended to select the desired delay time prior to power-on and not dynamically alter this selection.

See Calibration Feature for more information.

Power Down I-channel Pin (PDI)

The Power Down I-channel (PDI) Pin selects whether the I-channel is powered down (logic-high) or active (logiclow). The digital data output pins, DI and DId, (both positive and negative) are put into a high impedance state when the I-channel is powered down. Upon return to the active state, the pipeline will contain meaningless information and must be flushed. The supply currents (typicals and limits) are available for the I-channel powered down or active and may be found in Power Supply Characteristics. The device should be recalibrated following a power-cycle of PDI (or PDQ).

This pin remains active in ECM. In ECM, either this pin or the PDI bit (Addr: 0h; Bit: 11) in the Control Register may be used to power-down the I-channel. See Power Down for more information.

Power Down Q-channel Pin (PDQ)

The Power Down Q-channel (PDQ) Pin selects whether the Q-channel is powered down (logic-high) or active (logic-low). This pin functions similarly to the PDI pin, except that it applies to the Q-channel. The PDI and PDQ pins function independently of each other to control whether each I- or Q-channel is powered down or active.

This pin remains active in ECM. In ECM, either this pin or the PDQ bit (Addr: 0h; Bit: 10) in the Control Register may be used to power-down the Q-channel. See Power Down for more information.

Test Pattern Mode Pin (TPM)

The Test Pattern Mode (TPM) Pin selects whether the output of the B12D1000RH is a test pattern (logichigh) or the converted analog input (logic-low). The B12D1000RH can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In TPM, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. SeeTest Pattern Mode for more information.

Full-Scale Input Range Pin (FSR)

The Full-Scale Input Range (FSR) Pin selects whether the full-scale input range for both the I- and Q-channel is higher (logic-high) or lower (logic-low). The input full-scale range is specified as VIN_FSR in Analog Input/Output and Reference Characteristics. In Non-ECM, the full-scale input range for each I- and Q-channel may not be set independently, but it is possible to do so in ECM. The device must be calibrated following a change in FSR to obtain optimal performance.

To use this feature in ECM, use the Configuration Registers (Addr: 3h and Bh). See Input Control and Adjust for more information.

AC/DC-Coupled Mode Pin (V_{CMO})

The V_{CMO} Pin serves a dual purpose. When functioning as an output, it provides the optimal common-mode voltage for the DC-coupled analog inputs. When functioning as an input, it selects whether the device is AC-coupled (logic-low) or DC-coupled (floating). This pin is always active, in both ECM and Non-ECM.

LVDS Output Common-mode Pin (V_{BG})

The V_{BG} Pin serves a dual purpose. When functioning as an output, it provides the bandgap reference. When functioning as an input, it selects whether the LVDS output common-mode voltage is higher (logic-high) or lower (floating). The LVDS output common-mode voltage is specified as V_{OS} and may be found in Digital Control and Output Pin Characteristics. This pin is always active, in both ECM and Non-ECM.

Extended Control Mode

In Extended Control Mode (ECM), most functions are controlled via the Serial Interface. In addition to this, several of the control pins remain active. See Table 9-4 for details. ECM is selected by setting the ECE Pin to logic-low. If the ECE Pin is set to logic-high (Non-ECM), then the registers are reset to their default values. So, a simple way to reset the registers is by toggling the ECE pin. Four pins on the B12D1000RH control the Serial Interface: $\overline{SCS}$, SCLK, SDI and SDO. This section covers the Serial Interface. The Register Definitions are located at the end of the datasheet so that they are easy to find, see Register Definitions.

The Serial Interface

The B12D1000RH offers a Serial Interface that allows access to the sixteen control registers within the device. The Serial Interface is a generic 4-wire (optionally 3-wire) synchronous interface that is compatible with SPI type interfaces that are used on many micro-controllers and DSP controllers. Each serial interface access cycle is exactly 24 bits long. A register-read or register-write can be accomplished in one cycle. The signals are defined in such a way that the user can opt to simply join SDI and SDO signals in his system to accomplish a single, bidirectional SDI/O signal. A summary of the pins for this interface may be found in Table 9-2. See Figure 8-8 for the timing diagram and Serial Port Interface for timing specification details. Control register contents are retained when the device is put into power-down mode. If this feature is unused, the SCLK, SDI, and $\overline{SCS}$ pins may be left floating because they each have an internal pull-up.

Table 9-2 Serial Interface Pins

Pin Number	Pin Name
C4	$\overline{SCS}$(Serial Chip Select bar）
C5	SCLK（Serial Clock）
B4	SDI（Serial Data In）
A3	SDO（Serial Data Out）

$\overline{SCS}$: Each assertion (logic-low) of this signal starts a new register access, i.e. the SDI command field must be ready on the following SCLK rising edge. The user is required to de-assert this signal after the 24th clock. If the $\overline{SCS}$ is de-asserted before the 24th clock, no data read/write will occur. For a read operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, the SDO output will hold the D0 bit until $\overline{SCS}$ is de-asserted. For a write operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, data write will occur normally through the SDI input upon the 24th clock. Setup and hold times, t_{SCS} and t_{HCS}, with respect to the SCLK must be observed. $\overline{SCS}$ must be toggled in between register access cycles.

SCLK: This signal is used to register the input data (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. The user may disable the clock and hold it at logic-low. There is no minimum frequency requirement for SCLK; see f_{SCLK} in Serial Port Interface for more details.

SDI: Each register access requires a specific 24-bit pattern at this input, consisting of a command field and a data field. If the SDI and SDO wires are shared (3-wire mode), then during read operations, it is necessary to tristate the master which is driving SDI while the data field is being output by the ADC on SDO. The master must be at TRI-STATE before the falling edge of the 8th clock. If SDI and SDO are not shared (4-wire mode), then this is not necessary. Setup and hold times, t_{SH} and t_{SSU}, with respect to the SCLK must be observed.

SDO: This output is normally at TRI-STATE and is driven only when $\overline{SCS}$ is asserted, the first 8 bits of command data have been received and it is a READ operation. The data is shifted out, MSB first, starting with the 8^{th} clock's falling edge. At the end of the access, when $\overline{SCS}$ is de-asserted, this output is at TRI-STATE once again. If an invalid address is accessed, the data sourced will consist of all zeroes. If it is a read operation, there will be a bus turnaround time, t_{BSU}, from when the last bit of the command field was read in until the first bit of the data field is written out. Table 9-3 shows the Serial Interface bit definitions.

Table 9-3 Command and Data Field Definitions

Bit No.	Name	Comments
1	Read/Write(R/W)	1b indicates a read operation 0b indicates a write operation
2-3	Reserved	Bits must be set to 10b
4-7	A<3:0>	16 registers may be addressed. The order is MSB first
8	X	This is a “don’t care” bit
9-24	D<15:0>	Data written to or read from addressed register

The serial data protocol is shown for a read and write operation in Figure 9-1 and Figure 9-2, respectively.

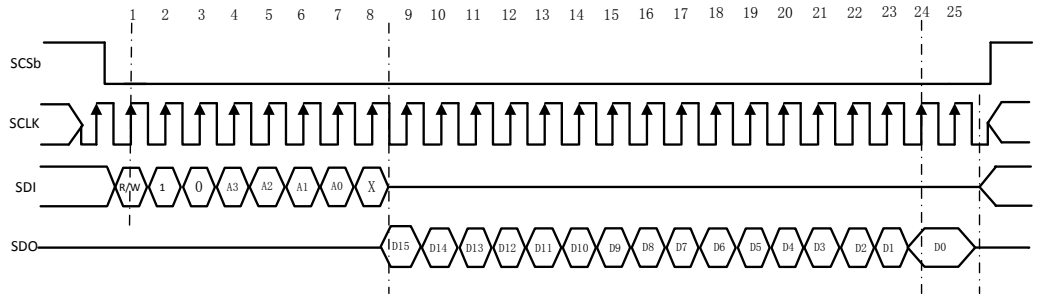


Figure 9-1. Serial Data protocol – Read Operation

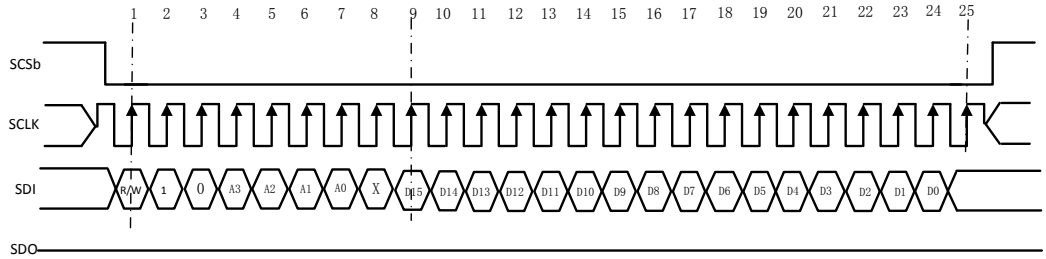


Figure 9-2. Serial Data protocol – Write Operation

9.3 Features

The B12D1000RH offers many features to make the device convenient to use in a wide variety of applications. Table 9-4 is a summary of the features available, as well as details for the control mode chosen. "N/A" means "Not Applicable."

Table 9-4 Features and Modes

Feature	Non-ECM	Control Pin Active in ECM	ECM	Default ECM State
Input Comtrol and Adjust				
AC/DC- coupled	Selected via	Yes	Not available	N/A

Mode Selection	V_{CMO} （Pin C2）			
Input Full-scale Range Adjust	Selected via FSR （Pin Y3）	No	Selected via the Config Reg （Addr:3h and Bh）	Mid FSR value
Input Offset Adjust Setting	Not available	N/A	Selected via the Config Reg （Addr:2h and Ah）	Offset=0mV
DES/Non-DES Mode Selection	Selected via DES （Pin V5）	No	Selected via the DES Bit （Addr:0h; Bit:7）	Non-DES Mode
DES Timing Adjust	Not available	N/A	Selected via the DES Timing Adjust Reg （Addr:7h）	Mid skew offset
Sampling Clock Phase Adjust	Not available	N/A	Selected via the Config Reg（Addr:Ch and Dh）	t_{AD} adjust disable
Output Control and Adjust				
DDR Clock Phase Selection	Selected via DDRPh（Pin W4）	No	Selected via DPS Bit （Addr:0h，Bit:14）	0 °Mode
LVDS Differential Voltage Amplitude Selection	Higher amplitude only	N/A	Selected via OVS Bit （Addr:0h，Bit:13）	High amplitude
LVDS Common-Mode Voltage Amplitude Selection	Selected via V_{BG} （Pin B1）	Yes	Not available	N/A
Output Formatting Selection	Offset Binary only	N/A	Selected via 2SC Bit （Addr:0h，Bit:4）	Offset Binary
Test Pattern Mode at Output	Selected via TPM （Pin A4）	No	Selected via TPM Bit （Addr:0h，Bit:12）	TPM disable
Demux/Non-Demux Mode Selection	Selected via NDM（Pin V5）	Yes	Not available	N/A
Auto Sync	Not available	N/A	Selected via the Config Reg （Addr:Eh）	Master Mode RCOut1/2 disabled
DCLK Reset	Not available	N/A	Selected via the Config Reg （Addr:Eh，Bit:0）	DCLK Reset disabled
Time Stamp	Not available	N/A	Selected via TSE Bit （Addr:0h，Bit:3）	Time Stamp disabled

Calibration				
On-command Calibration	Selected via CAL（Pin D6）	Yes	Selected via CAL Bit（Addr:0h，Bit:15）	N/A(CAL=0)
Power-on Calibration Delay Selection	Selected via CalDly（Pin V4）	Yes	Not available	N/A
Calibration Adjust	Not available	N/A	elected via the Config Reg（Addr:4h）	t_{CAL}
Read/Write Calibration Settings	Not available	N/A	Selected via SSC Bit（Addr:4h，Bit:7）	R/W calibration values disabled
Power-Down				
Power down I-channel	Selected via PDI（Pin U3）	Yes	Selected via PDI Bit（Addr:0h，Bit:11）	I-channel operational
Power down Q-channel	Selected via PDQ（Pin V3）	Yes	Selected via PDQ Bit（Addr:0h，Bit:10）	Q-channel operational

Input Control and Adjust

There are several features and configurations for the input of the B12D1000RH so that it may be used in many different applications. This section covers AC/DC-coupled Mode, input full-scale range adjust, input offset adjust, DES/Non-DES Mode, and sampling clock phase adjust.

AC/DC-coupled Mode

The analog inputs may be AC or DC-coupled. See AC/DC-Coupled Mode Pin (V_{CMO}) for information on how to select the desired mode and DC-coupled Input Signals and AC-coupled Input Signals for applications information.

Input Full-Scale Range Adjust

The input full-scale range for the B12D1000RH may be adjusted via Non-ECM or ECM. In Non-ECM, a control pin selects a higher or lower value; see Full-Scale Input Range Pin (FSR). In ECM, the input full-scale range may be adjusted with 15-bits of precision. See V_{IN_FSR} in Analog Input/Output and Reference Characteristics for electrical specification details. Note that the higher and lower full-scale input range settings in Non-ECM correspond to the mid and min full-scale input range settings in ECM. It is necessary to execute an on-command calibration following a change of the input full-scale range. See Register Definitions for information about the registers.

Input Offset Adjust

The input offset adjust for the B12D1000RH may be adjusted with 12-bits of precision plus sign via ECM. See Register Definitions for information about the registers.

DES/Non-DES Mode

The B12D1000RH can operate in Dual-Edge Sampling (DES) or Non-DES Mode. The DES Mode allows for a single analog input to be sampled by both I- and Q-channels. One channel samples the input on the rising edge of the sampling clock and the other samples the same input signal on the falling edge of the sampling clock. A single input is thus sampled twice per clock cycle, resulting in an overall sample rate of twice the sampling clock frequency, e.g. 2.0 GSPS with a 1.0 GHz sampling clock. Since DES Mode uses both Iand Q-channels to process the input signal, both channels must be powered up for the DES Mode to function properly.

In Non-ECM, only the I-input may be used for the DES Mode input. See Dual Edge Sampling Pin (DES) for information on how to select the DES Mode. In ECM, either the I- or Q-input may be selected by first using the DES bit (Addr: 0h, Bit 7) to select the DES Mode. The DEQ Bit (Addr: 0h, Bit: 6) is used to select the Q-input, but the I-input is used by default. Also, both I- and Q-inputs may be driven externally, i.e. DESIQ Mode, by using the DIQ bit (Addr: 0h, Bit 5). See Driving the ADC in DES Mode for more information about how to drive the ADC in DES Mode.

The DESIQ Mode results in the best DES Mode bandwidth. In general, the bandwidth decreases from Non-DES Mode to DES Mode (specifically, DESI or DESQ) because both channels are sampling off the same input signal and non-ideal effects introduced by interleaving the two channels lower the bandwidth. Driving both I- and Qchannels externally (DESIQ Mode) results in better bandwidth for the DES Mode because each channel is being driven, which reduces routing losses.

In the DES Mode, the outputs must be carefully interleaved in order to reconstruct the sampled signal. If the device is programmed into the 1:4 Demux DES Mode, the data is effectively demultiplexed by 1:4. If the sampling clock is 1.0 GHz, the effective sampling rate is doubled to 2.0 GSPS and each of the 4 output buses has an output rate of 500/800 MSPS. All data is available in parallel. To properly reconstruct the sampled waveform, the four bytes of parallel data that are output with each DCLK must be correctly interleaved. The sampling order is as follows, from the earliest to the latest: DQd, DId, DQ, DI. See Figure 8-4. If the device is programmed into the Non-Demux DES Mode, two bytes of parallel data are output with each edge of the DCLK in the following sampling order, from the earliest to the latest: DQ, DI. See Figure 8-5.

DES Timing Adjust

The performance of the B12D1000RH in DES Mode depends on how well the two channels are interleaved, i.e. that the clock samples either channel with precisely a

50% duty-cycle, each channel has the same offset (nominally code 2047/2048), and each channel has the same full-scale range. The B12D1000RH includes an automatic clock phase background adjustment in DES Mode to automatically and continuously adjust the clock phase of the I- and Q-channels. In addition to this, the residual fixed timing skew offset may be further manually adjusted, and further reduce timing spurs for specific applications. See the DES Timing Adjust (Addr: 7h). As the DES Timing Adjust is programmed from 0d to 127d, the magnitude of the Fs/2-Fin timing interleaving spur will decrease to a local minimum and then increase again. The default, nominal setting of 64d may or may not coincide with this local minimum. The user may manually skew the global timing to achieve the lowest possible timing interleaving spur.

Sampling Clock Phase Adjust

The sampling clock (CLK) phase may be delayed internally to the ADC up to 825 ps in ECM. This feature is intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used, or to simplify complex system functions such as beam steering for phase array antennas.

Additional delay in the clock path also creates additional jitter when using the sampling clock phase adjust. Because the sampling clock phase adjust delays all clocks, including the DCLKs and output data, the user is strongly advised to use the minimal amount of adjustment and verify the net benefit of this feature in his system before relying on it.

Output Control and Adjust

There are several features and configurations for the output of the B12D1000RH so that it may be used in many different applications. This section covers DDR clock phase, LVDS output differential and common-mode voltage, output formatting, Demux/Non-demux Mode, Test Pattern Mode, and Time Stamp.

DDR Clock Phase

The B12D1000RH output data is always delivered in Double Data Rate (DDR). With DDR, the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK; see Figure 9-3. The DCLK-to-Data phase relationship may be either 0 ° or 90 °. For 0 ° Mode, the Data transitions on each edge of the DCLK. Any offset from this timing is tOSK; see AC Electrical Characteristics for details. For 90 ° Mode, the DCLK transitions in the middle of each Data cell. Setup and hold times for this transition, tSU and tH, may also be found in AC Electrical Characteristics . The

DCLK-to-Data phase relationship may be selected via the DDRPh Pin in Non-ECM (see Dual Data Rate Phase Pin (DDRPh)) or the DPS bit in the Configuration Register (Addr: 0h; Bit: 14) in ECM.

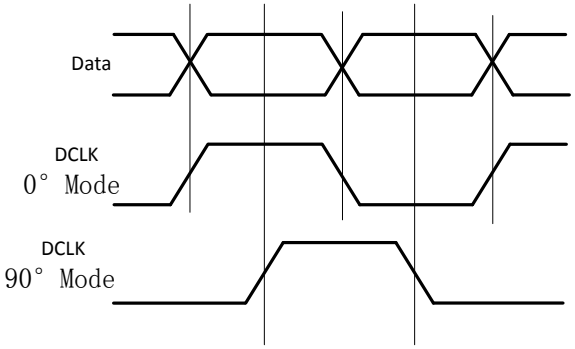


Figure 9-3. DDR DCLK-to-Data Phase Relationship

LVDS Output Differential Voltage

The B12D1000RH is available with a selectable higher or lower LVDS output differential voltage. This parameter is VOD and may be found in Digital Control and Output Pin Characteristics. The desired voltage may be selected via the OVS Bit (Addr: 0h, Bit 13). For many applications, in which the LVDS outputs are very close to an FPGA on the same board, for example, the lower setting is sufficient for good performance; this will also reduce the possibility for EMI from the LVDS outputs to other signals on the board. See Register Definitions for more information.

LVDS Output Common-Mode Voltage

The B12D1000RH is available with a selectable higher or lower LVDS output common-mode voltage. This parameter is V_{OS} and may be found in Digital Control and Output Pin Characteristics. See LVDS Output Common-mode Pin (V_{BG}) for information on how to select the desired voltage.

Output Formatting

The formatting at the digital data outputs may be either offset binary or two's complement. The default formatting is offset binary, but two's complement may be selected via the 2SC Bit (Addr: 0h, Bit 4); see Register Definitions for more information.

Demux/Non-demux Mode

The B12D1000RH may be in one of two demultiplex modes: Demux Mode or Non-Demux Mode (also sometimes referred to as 1:1 Demux Mode). In Non-Demux Mode, the data from the input is simply output at the sampling rate on one 12-bit bus. In Demux Mode, the data from the input is output at half the sampling rate, on twice the number of buses. Demux/Non-Demux Mode may only be selected by the NDM

pin. In Non-DES Mode, the output data from each channel may be demultiplexed by a factor of 1:2 (1:2 Demux Non-DES Mode) or not demultiplexed (Non-Demux Non-DES Mode). In DES Mode, the output data from both channels interleaved may be demultiplexed (1:4 Demux DES Mode) or not demultiplexed (Non-Demux DES Mode).

Test Pattern Mode

The B12D1000RH can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In Test Pattern Mode, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. The test pattern output is the same in DES Mode or Non-DES Mode. Each port is given a unique 12-bit word, alternating between 1's and 0's. When the part is programmed into the Demux Mode, the test pattern's order is described in Table 9-5. If the I- or Q-channel is powered down, the test pattern will not be output for that channel.

Table 9-5 Test Pattern by Output Port in Demux Mode

Time	Qd	Id	Q	I	ORQ	ORI	Comments
T0	000h	004h	008h	010h	0b	0b	Pattern Sequence n
T1	FFFh	FFBh	FF7h	FEFh	1b	1b	
T2	000h	004h	008h	010h	0b	0b	
T3	FFFh	FFBh	FF7h	FEFh	1b	1b	
T4	000h	004h	008h	010h	0b	0b	
T5	000h	004h	008h	010h	0b	0b	Pattern Sequence n+1
T6	FFFh	FFBh	FF7h	FEFh	1b	1b	
T7	000h	004h	008h	010h	0b	0b	
T8	FFFh	FFBh	FF7h	FEFh	1b	1b	
T9	000h	004h	008h	010h	0b	0b	
T10	000h	004h	008h	010h	0b	0b	Pattern Sequence n+2
T11	FFFh	FFBh	FF7h	FEFh	1b	1b	
T12	000h	004h	008h	010h	0b	0b	
T13	…	…	…	…	…	…	

When the part is programmed into the Non-Demux Mode, the test pattern's order is described in Table 9-6.

Table 9-6 Test Pattern by Output Port in Non-Demux Mode

Time	Q	I	ORQ	ORI	Comments
T0	000h	004h	0b	0b	

T1	000h	004h	0b	0b	Pattern Sequence n
T2	FFFh	FFBh	1b	1b	
T3	FFFh	FFBh	1b	1b	
T4	000h	004h	0b	0b	
T5	FFFh	FFBh	1b	1b	
T6	000h	004h	0b	0b	
T7	FFFh	FFBh	1b	1b	
T8	FFFh	FFBh	1b	1b	
T9	FFFh	FFBh	1b	1b	
T10	000h	004h	0b	0b	Pattern Sequence n+1
T11	000h	004h	0b	0b	
T12	FFFh	FFBh	1b	1b	
T13	FFFh	FFBh	1b	1b	
T14	…	…	…	…	

Time Stamp

The Time Stamp feature enables the user to capture the timing of an external trigger event, relative to the sampled signal. When enabled via the TSE Bit (Addr: 0h; Bit: 3), the LSB of the digital outputs (DQd, DQ, DId, DI) captures the trigger information. In effect, the 12-bit converter becomes an 11-bit converter and the LSB acts as a 1-bit converter with the same latency as the 11-bit converter. The trigger should be applied to the DCLK_RST input. It may be asynchronous to the ADC sampling clock.

Calibration Feature

The B12D1000RH calibration must be run to achieve specified performance. The calibration procedure is exactly the same regardless of how it was initiated or when it is run. Calibration trims the analog input differential termination resistors, the CLK input resistor, and sets internal bias currents which affect the linearity of the converter. This minimizes full-scale error, offset error, DNL and INL, which results in the maximum dynamic performance, as measured by: SNR, THD, SINAD (SNDR) and ENOB.

Calibration Control Pins and Bits

Table 9-7 is a summary of the pins and bits used for calibration. See Ball Descriptions and Equivalent Circuits for complete pin information and Figure 8-7 for the timing diagram.

Table 9-7 Calibration Pins

Pin（Bit）	Name	Function
D6（Addr：0h，Bit15）	CAL（Calibration）	Initiate calibration
V4	CalDly（Calibration Delay）	Select power-on calibration delay
（Addr:4h）	Calibration Adjust	Adjust calibration sequence
B5	CalRun（Calibration Running）	Indicates while calibration is running
C1/D2	Rtrim+/-（(Input termination trim resistor）	External resistor used to calibrate analog and CLK inputs
C3/D3	Rext+/-（External Reference resistor）	External resistor used to calibrate internal linearity

How to Execute a Calibration

Calibration may be initiated by holding the CAL pin low for at least t_{CAL_L} clock cycles, and then holding it high for at least another t_{CAL_H} clock cycles, as defined in Calibration. The minimum t_{CAL_L} and t_{CAL_H} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. The time taken by the calibration procedure is specified as t_{CAL}. The CAL Pin is active in both ECM and Non-ECM. However, in ECM, the CAL Pin is logically OR'd with the CAL Bit, so both the pin and bit are required to be set low before executing another calibration via either pin or bit.

Power-on Calibration

For standard operation, power-on calibration begins after a time delay following the application of power, as determined by the setting of the CalDly Pin and measured by t_{CalDly} (see Calibration). This delay allows the power supply to come up and stabilize before the power-on calibration takes place. The best setting (short or long) of the CalDly Pin depends upon the settling time of the power supply.

It is strongly recommended to set CalDly Pin (to either logic-high or logic-low) before powering the device on since this pin affects the power-on calibration timing. This may be accomplished by setting CalDly via an external 1kΩ resistor connected to GND or V_A. If the CalDly Pin is toggled while the device is powered-on, it can execute a calibration even though the CAL Pin/Bit remains logic-low.

The power-on calibration will be not be performed if the CAL pin is logic-high at power-on. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The B12D1000RH will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired.

If it is necessary to toggle the CalDly Pin before the system power up sequence, then the CAL Pin/Bit must be set to logic-high during the toggling and afterwards for

10^9 Sampling Clock cycles. This will prevent the power-on calibration, so an on-command calibration must be executed or the performance will be impaired.

On-command Calibration

In addition to the power-on calibration, it is recommended to execute an on-command calibration whenever the settings or conditions to the device are altered significantly, in order to obtain optimal parametric performance. Some examples include: changing the FSR via either ECM or Non-ECM, power-cycling either channel, and switching into or out of DES Mode. For best performance, it is also recommended that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, relative to the specific system performance requirements.

Due to the nature of the calibration feature, it is recommended to avoid unnecessary activities on the device while the calibration is taking place. For example, do not read or write to the Serial Interface or use the DCLK Reset feature while calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Also, it is recommended to not apply a strong narrow-band signal to the analog inputs during calibration because this may impair the accuracy of the calibration; broad spectrum noise is acceptable.

Calibration Adjust

The sequence of the calibration event itself may be adjusted. This feature can be used if a shorter calibration time than the default is required; see t_{CAL} in Calibration. However, the performance of the device, when using this feature is not ensured.

The calibration sequence may be adjusted via CSS (Addr: 4h, Bit 14). The default setting of CSS = 1b executes both RIN and RIN_CLK Calibration (using Rtrim) and internal linearity Calibration (using Rext). Executing a calibration with CSS = 0b executes only the internal linearity Calibration. The first time that Calibration is executed, it must be with CSS = 1b to trim RIN and RIN_CLK. However, once the device is at its operating temperature and RIN has been trimmed at least one time, it will not drift significantly. To save time in subsequent calibrations, trimming RIN and RIN_CLK may be skipped, i.e. by setting CSS = 0b.

Read/Write Calibration Settings

When the ADC performs a calibration, the calibration constants are stored in an array which is accessible via the Calibration Values register (Addr: 5h). To save the time which it takes to execute a calibration, t_{CAL}, or to allow re-use of a previous calibration result, these values can be read from and written to the register at a later

time. For example, if an application requires the same input impedance, R_{IN}, this feature can be used to load a previously determined set of values. For the calibration values to be valid, the ADC must be operating under the same conditions, including temperature, at which the calibration values were originally determined by the ADC.

To read calibration values from the SPI, do the following:

1. Set ADC to desired operating conditions.
2. Set SSC (Addr: 4**h**, Bit 7) to 1.
3. Read exactly 240 times the Calibration Values register (Addr: 5**h**). The register values are R0, R1, R2... R239 where R0 is adummy value. The contents of R<239:1> should be stored.
4. Set SSC (Addr: 4**h**, Bit 7) to 0.
5. Continue with normal operation.

To write calibration values to the SPI, do the following:

1. Set ADC to operating conditions at which Calibration Values were previously read.
2. Set SSC (Addr: 4**h**, Bit 7) to 1.
3. Write exactly 239 times the Calibration Values register (Addr: 5**h**). The registers should be written with stored register valuesR1, R2... R239.
4. Make two additional dummy writes of 0000**h**.
5. Set SSC (Addr: 4**h**, Bit 7) to 0.
6. Continue with normal operation.

Calibration and Power-Down

If PDI and PDQ are simultaneously asserted during a calibration cycle, the B12D1000RH will immediately power down. The calibration cycle will continue when either or both channels are powered back up, but the calibration will be compromised due to the incomplete settling of bias currents directly after power up. Therefore, a new calibration should be executed upon powering the B12D1000RH back up. In general, the B12D1000RH should be recalibrated when either or both channels are powered back up, or after one channel is powered down. For best results, this should be done after the device has stabilized to its operating temperature.

Calibration and the Digital Outputs

During calibration, the digital outputs (including DI, DId, DQ, DQd and OR) are set logic-low, to reduce noise. The DCLK runs continuously during calibration. After the calibration is completed and the CalRun signal is logiclow, it takes an additional 60 Sampling Clock cycles before the output of the B12D1000RH is valid converted data from the analog inputs. This is the time it takes for the pipeline to flush, as well

as for other internal processes.

Power Down

On the B12D1000RH, the I- and Q-channels may be powered down individually. This may be accomplished via the control pins, PDI and PDQ, or via ECM. In ECM, the PDI and PDQ pins are logically OR'd with the Control Register setting. See Power Down I-channel Pin (PDI) andPower Down Q-channel Pin (PDQ) for more information.

9.4 Applications Information

THE ANALOG INPUTS

The B12D1000RH will continuously convert any signal which is present at the analog inputs, as long as a CLK signal is also provided to the device. This section covers important aspects related to the analog inputs including: acquiring the input, driving the ADC in DES Mode, the reference voltage and FSR, out-of-range indication, AC/DC-coupled signals, and single-ended input signals.

Acquiring the Input

Data is acquired at the rising edge of CLK+ in Non-DES Mode and both the falling and rising edges of CLK+ in DES Mode. The digital equivalent of that data is available at the digital outputs a constant number of sampling clock cycles later for the DI, DQ, DId and DQd output buses, a.k.a. Latency, depending on the demultiplex mode which is selected. See tLAT in AC Electrical Characteristics . In addition to the Latency, there is a constant output delay, t_{OD}, before the data is available at the outputs. See t_{OD} in AC Electrical Characteristics and the Timing Diagrams.

The output latency versus Demux/Non-Demux Mode is shown in Table 9-8 and Table 9-9, respectively. For DES Mode, note that the I- and Q-channel inputs are available in ECM, but only the I-channel input is available in Non-ECM.

Table 9-8 Output Latency in Demux Mode

Data	Non-Des Mode	DES Mode	
		Q-input*	I-input
DI	I-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with rise of CLK, 34 cycles earlier	I-input sampled with rise of CLK, 34 cycles earlier
DQ	Q-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with fall of CLK, 34.5 cycles earlier	I-input sampled with fall of CLK, 34.5 cycles earlier
DId	I-input sampled with rise of CLK, 35 cycles	Q-input sampled with rise of CLK, 35 cycles	I-input sampled with rise of CLK, 35 cycles

	earlier	earlier	earlier
DQd	Q-input sampled with rise of CLK, 35 cycles earlier	Q-input sampled with fall of CLK, 35.5 cycles earlier	I-input sampled with fall of CLK, 35.5 cycles earlier

Table 9-9 Output Latency in Non-Demux Mode

Data	Non-Des Mode	DES Mode	
		Q-input*	I-input
DI	I-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with rise of CLK, 34 cycles earlier	I-input sampled with rise of CLK, 34 cycles earlier
DQ	Q-input sampled with rise of CLK, 34 cycles earlier	Q-input sampled with rise of CLK, 34.5 cycles earlier	I-input sampled with rise of CLK, 34.5 cycles earlier
DId	No output, high impedance.		
DQd	No output, high impedance.		

Note：*Available in ECM only.

Driving the ADC in DES Mode

The B12D1000RH can be configured as either a 2-channel, 1.0GSPS device (Non-DES Mode) or a 1-channel 2.0GSPS device (DES Mode). When the device is configured in DES Mode, there is a choice for with which input to drive the single-channel ADC. These are the 3 options:

DES – externally driving the I-channel input only. This is the default selection when the ADC is configured in DES Mode. It may also be referred to as “DESI” for added clarity.

DESQ – externally driving the Q-channel input only.

DESIQ – externally driving both the I- and Q-channel inputs. VinI+ and VinQ+ should be driven with the exact same signal. VinI- and VinQ- should be driven with the exact same signal, which is the differential complement to the one driving VinI+ and VinQ+.

The input impedance for each I- and Q-input is 100Ω differential (or 50Ω single-ended), so the trace to each VinI+, VinI-, VinQ+, and VinQ- should always be 50Ω single-ended. If a single I- or Q-input is being driven, then that input will present a 100Ω differential load. For example, if a 50Ω single-ended source is driving the ADC, then a 1:2 balun will transform the impedance to 100Ω differential. However, if the ADC is being driven in DESIQ Mode, then the 100Ω differential impedance from the I-input will appear in parallel with the Q-input for a composite load of 50Ω differential and a 1:1 balun would be appropriate. See Figure 9-4 for an

example circuit driving the ADC in DESIQ Mode.

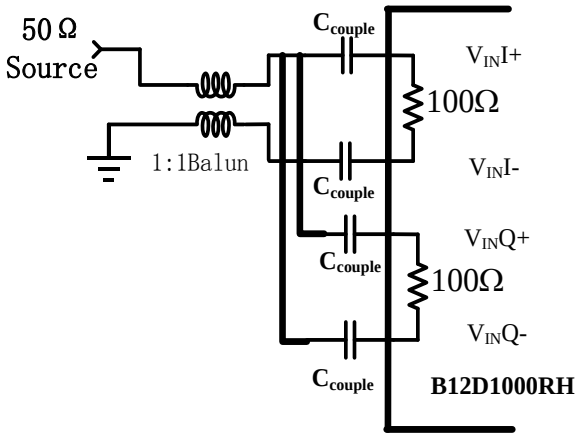


Figure 9-4. Driving DESIQ Mode

In the case that only one channel is used in Non-DES Mode or that the ADC is driven in DESI or DESQ Mode, the unused analog input should be terminated to reduce any noise coupling into the ADC. See Table 9-10 for details.

Table 9-10 Unused Analog Input Recommended Termination

Mode	Power Down	Coupling	Recommended Termination
Non-DES	Yes	AC/DC	Tie Unused+ and Unused- to Vbg
DES/Non-DES	No	DC	Tie Unused+ and Unused- to Vbg
DES/Non-DES	No	AC	Tie Unused+ to Unused-

FSR and the Reference Voltage

The full-scale analog differential input range (V_{IN_FSR}) of the B12D1000RH is derived from an internal bandgap reference. In Non-ECM, this full-scale range has two settings controlled by the FSR Pin; see Full-Scale Input Range Pin (FSR). The FSR Pin operates on both I- and Q-channels. In ECM, the full-scale range may be independently set for each channel via Addr:3h and Bh with 15 bits of precision; see Register Definitions. The best SNR is obtained with a higher full-scale input range, but better distortion and SFDR are obtained with a lower full-scale input range. It is not possible to use an external analog reference voltage to modify the full-scale range, and this adjustment should only be done digitally, as described.

A buffered version of the internal bandgap reference voltage is made available at the V_{BG} Pin for the user. The V_{BG} pin can drive a load of up to 80 pF and source or sink up to 100 μ A. It should be buffered if more current than this is required. This pin remains as a constant reference voltage regardless of what full-scale range is selected and may be used for a system reference. V_{BG} is a dual-purpose pin and it may also be used to select a higher LVDS output common-mode voltage; see LVDS Output Common-mode Pin (V_{BG}).

Out-Of-Range Indication

Differential input signals are digitized to 12 bits, based on the full-scale range. Signal excursions beyond the fullscale range, i.e. greater than $+V_{IN\_FSR/2}$ or less than $-V_{IN\_FSR/2}$, will be clipped at the output. An input signal which is above the FSR will result in all 1's at the output and an input signal which is below the FSR will result in all 0's at the output. When the conversion result is clipped for the I-channel input, the Out-of-Range I-channel (ORI) output is activated such that ORI+ goes high and ORI- goes low while the signal is out of range. This output is active as long as accurate data on either or both of the buses would be outside the range of 000h to FFFh. The Q-channel has a separate ORQ which functions similarly.

Maximum Input Range

The recommended operating and absolute maximum input range may be found in Operating Ratings and Absolute Maximum Ratings, respectively. Under the stated allowed operating conditions, each Vin+ and Vininput pin may be operated in the range from 0V to 2.15V if the input is a continuous 100% duty cycle signal and from 0V to 2.5V if the input is a 10% duty cycle signal. The absolute maximum input range for Vin+ and Vin- is from -0.15V to 2.5V. These limits apply only for input signals for which the input common mode voltage is properly maintained.

AC-coupled Input Signals

The B12D1000RH analog inputs require a precise common-mode voltage. This voltage is generated onchip when AC-coupling Mode is selected. See AC/DC-Coupled Mode Pin (V_{CMO}) for more information about how to select AC-coupled Mode.

In AC-coupled Mode, the analog inputs must of course be AC-coupled. For an B12D1000RH used in a typical application, this may be accomplished by on-board capacitors, as shown in Figure 9-5.

When the AC-coupled Mode is selected, an analog input channel that is not used (e.g. in DES Mode) should be connected to AC ground, e.g. through capacitors to ground . Do not connect an unused analog input directly to ground.

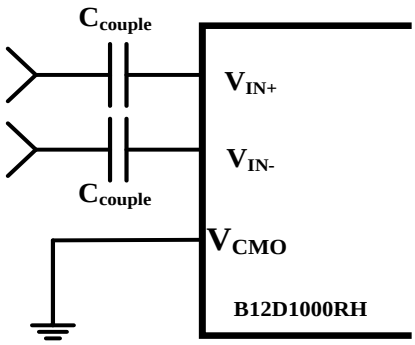


Figure 9-5. AC-coupled Differential Input

The analog inputs for the B12D1000RH are internally buffered, which simplifies the task of driving these inputs and the RC pole which is generally used at sampling ADC inputs is not required. If the user desires to place an amplifier circuit before the ADC, care should be taken to choose an amplifier with adequate noise and distortion performance, and adequate gain at the frequencies used for the application.

DC-coupled Input Signals

In DC-coupled Mode, the B12D1000RH differential inputs must have the correct common-mode voltage. This voltage is provided by the device itself at the V_{CMO} output pin. It is recommended to use this voltage because the V_{CMO} output potential will change with temperature and the common-mode voltage of the driving device should track this change. Full-scale distortion performance falls off as the input common mode voltage deviates from V_{CMO}. Therefore, it is recommended to keep the input common-mode voltage within 100 mV of V_{CMO} (typical), although this range may be extended to ±150 mV (maximum). See VCMI in Analog Input/Output and Reference Characteristics and ENOB vs. V_{CMI} in Typical Performance Plots . Performance in AC- and DCcoupled Mode are similar, provided that the input common mode voltage at both analog inputs remains within 100 mV of V_{CMO}.

Single-Ended Input Signals

The analog inputs of the B12D1000RH are not designed to accept single-ended signals. The best way to handle single-ended signals is to first convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-transformer, as shown in Figure 9-6.

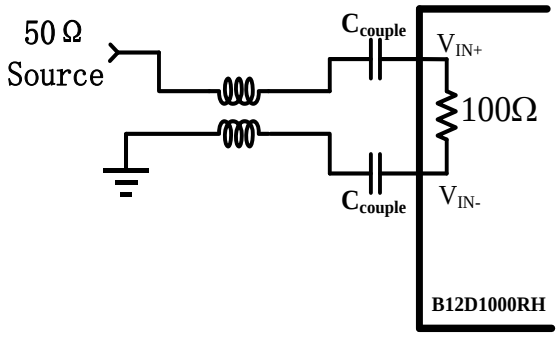


Figure 9-6. Single-Ended to Differential Conversion Using a Balun

When selecting a balun, it is important to understand the input architecture of the ADC. The impedance of the analog source should be matched to the B12D1000RH's on-chip 100Ω differential input termination resistor. The range of this termination resistor is specified as RIN in Analog Input/Output and Reference Characteristics.

THE CLOCK INPUTS

The B12D1000RH has a differential clock input, CLK+ and CLK-, which must be driven with an AC-coupled, differential clock signal. The clock inputs are internally terminated to 100Ω differential and selfbiased. This section covers coupling, frequency range, level, duty-cycle, jitter, and layout considerations.

CLK Coupling

The clock inputs of the B12D1000RH must be capacitively coupled to the clock pins as indicated in Figure 9-7.

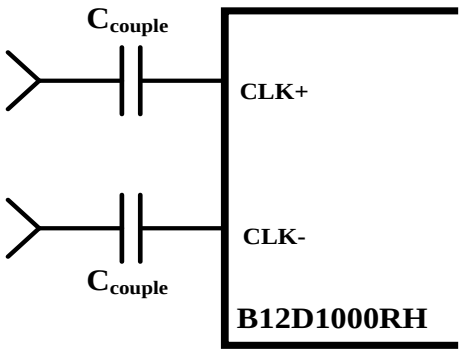


Figure 9-7. Differential Input Clock Connection

The choice of capacitor value will depend on the clock frequency, capacitor component characteristics and other system economic factors. For example, on the B12D1000RH Evaluation Board, the capacitors have the value C_{couple} = 4.7 nF which yields a highpass cutoff frequency, f_c = 677.2 kHz.

CLK Frequency

Although the B12D1000RH is tested and its performance is ensured with a differential 1.0 GHz sampling clock, it will typically function well over the input clock frequency range; see $f_{CLK(min)}$ and $f_{CLK(max)}$ in AC Electrical Characteristics . Operation up to f_{CLK}(max) is possible if the maximum ambient temperatures indicated are not exceeded. Operating at sample rates above $f_{CLK(max)}$ for the maximum ambient temperature may result in reduced device reliability and product lifetime. This is due to the fact that higher sample rates results in higher power consumption and die temperatures. If f_{CLK} < 300 MHz, enable LFS in the Control Register (Addr: 0h, Bit 8).

CLK Level

The input clock amplitude is specified as V_{IN_CLK} in Converter Electrical Characteristics Sampling Clock Characteristics . Input clock amplitudes above the max V_{IN_CLK} may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 2047/2048 when both input pins are at the same potential. Insufficient input clock levels will result in poor dynamic performance. Both of these results may be avoided by keeping the clock input amplitude within the specified limits of V_{IN_CLK}.

CLK Duty Cycle

The duty cycle of the input clock signal can affect the performance of any A/D converter. The B12D1000RH features a duty cycle clock correction circuit which can maintain performance over the 20%-to-80% specified clock duty-cycle range. This feature is enabled by default and provides improved ADC clocking, especially in the Dual-Edge Sampling (DES) Mode.

CLK Jitter

High speed, high performance ADCs such as the B12D1000RH require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)} / V_{FSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

Where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{FSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC

analog input.

$t_{J(MAX)}$ is the square root of the sum of the squares (RSS) of the jitter from all sources, including: the ADC input clock, system, input signals and the ADC itself. Since the effective jitter added by the ADC is beyond user control, it is recommended to keep the sum of all other externally added jitter to a minimum.

CLK Layout

The B12D1000RH clock input is internally terminated with a trimmed 100Ω resistor. The differential input clock line pair should have a characteristic impedance of 100Ω and (when using a balun), be terminated at the clock source in that (100Ω) characteristic impedance.

It is good practice to keep the ADC input clock line as short as possible, tightly coupled, keep it well away from any other signals, and treat it as a transmission line. Otherwise, other signals can introduce jitter into the input clock signal. Also, the clock signal can introduce noise into the analog path if it is not properly isolated.

THE LVDS OUTPUTS

The Data, ORI, ORQ, DCLKI and DCLKQ outputs are LVDS. The electrical specifications of the LVDS outputs are compatible with typical LVDS receivers available on ASIC and FPGA chips; but they are not IEEE or ANSI communications standards compliant due to the low +1.9V supply used on this chip. These outputs should be terminated with a 100Ω differential resistor placed as closely to the receiver as possible. If the 100Ω differential resistance is built in to the receiver, then an externally placed resistor is not necessary. This section covers common-mode and differential voltage, and data rate.

Common-mode and Differential Voltage

The LVDS outputs have selectable common-mode and differential voltage, V_{OS} and V_{OD}; see Digital Control and Output Pin Characteristics. See Output Control and Adjust for more information. Selecting the higher V_{OS} will also increase V_{OD} slightly. The differential voltage, V_{OD}, may be selected for the higher or lower value. For short LVDS lines and low noise systems, satisfactory performance may be realized with the lower V_{OD}. This will also result in lower power consumption. If the LVDS lines are long and/or the system in which the B12D1000RH is used is noisy, it may be necessary to select the higher V_{OD}.

Output Data Rate

The data is produced at the output at the same rate it is sampled at the input. The minimum recommended input clock rate for this device is $f_{CLK(MIN)}$; see AC Electrical

Characteristics . However, it is possible to operate the device in 1:2 Demux Mode and capture data from just one 12-bit bus, e.g. just DI (or DId) although both DI and DId are fully operational. This will decimate the data by two and effectively halve the data rate.

Terminating Unused LVDS Output Pins

If the ADC is used in Non-Demux Mode, then only the DI and DQ data outputs will have valid data present on them. The DId and DQd data outputs may be left not connected; if unused, they are internally at TRI-STATE. Similarly, if the Q-channel is powered-down (i.e. PDQ is logic-high), the DQ data output pins, DCLKQ and ORQ may be left not connected.

SYNCHRONIZING MULTIPLE B12D1000RH IN A SYSTEM

The B12D1000RH has two features to assist the user with synchronizing multiple ADCs in a system; AutoSync and DCLK Reset. The AutoSync feature is new and designates one B12D1000RH as the Master ADC and other B12D1000RH in the system as Slave ADCs. The DCLK Reset feature performs the same function as the AutoSync feature, but is the first generation solution to synchronizing multiple ADCs in a system; it is disabled by default. For the application in which there are multiple Master and Slave B12D1000RH in a system, AutoSync may be used to synchronize the Slave B12D1000RH to each respective Master B12D1000RH and the DCLK Reset may be used to synchronize the Master B12D1000RH to each other.

If the AutoSync or DCLK Reset feature is not used, see Table 9-11 for recommendations about terminating unused pins.

Table 9-11 Unused AutoSync and DCLK Reset Pin Recommendation

Pin(s)	Unused termination
RCLK+/-	Do not connect
RCOUT1+/-	Do not connect
RCOUT2+/-	Do not connect
DCLK_RST+	Connect to GND via 1kΩ resistor
DCLK_RST-	Connect to VA via 1kΩ resistor.

AutoSync Feature

AutoSync is a new feature which continuously synchronizes the outputs of multiple B12D1000RH in a system. It may be used to synchronize the DCLK and data outputs of one or more Slave B12D1000RH to one Master B12D1000RH. Several advantages of this feature include: no special synchronization pulse required, any upset in synchronization is recovered upon the next DCLK cycle, and the Master/Slave B12D1000RH may be arranged as a binary tree so that any upset will quickly

propagate out of the system.

An example system is shown below in Figure 9-8 which consists of one Master ADC and two Slave ADCs. For simplicity, only one DCLK is shown; in reality, there is DCLKI and DCLKQ, but they are always in phase with one another.

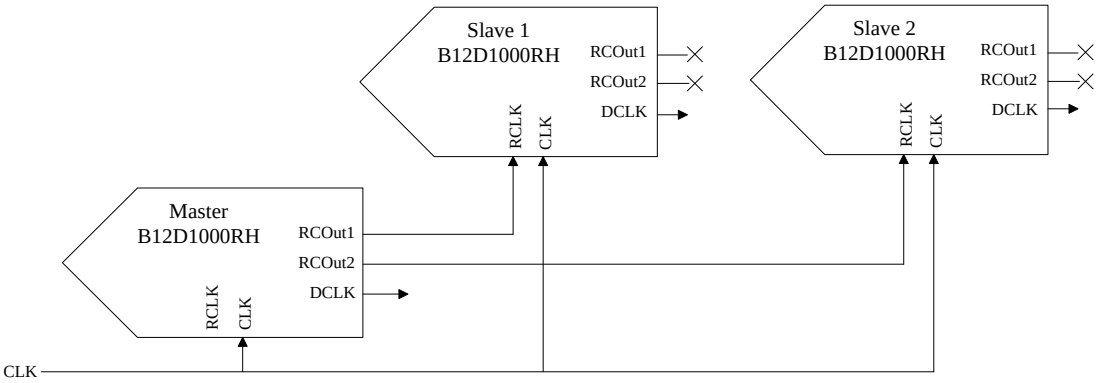


Figure 9-8 AutoSync Example

In order to synchronize the DCLK (and Data) outputs of multiple ADCs, the DCLKs must transition at the same time, as well as be in phase with one another. The DCLK at each ADC is generated from the CLK after some latency, plus t_{OD} minus t_{AD}. Therefore, in order for the DCLKs to transition at the same time, the CLK signal must reach each ADC at the same time. To tune out any differences in the CLK path to each ADC, the t_{AD} adjust feature may be used. However, using the t_{AD} adjust feature will also affect when the DCLK is produced at the output. If the device is in Demux Mode, then there are four possible phases which each DCLK may be generated on because the typical CLK = 1GHz and DCLK = 250 MHz for this case. The RCLK signal controls the phase of the DCLK, so that each Slave DCLK is on the same phase as the Master DCLK. The AutoSync feature may only be used via the Control Registers.

DCLK Reset Feature

The DCLK reset feature is available via ECM, but it is disabled by default. DCLKI and DCLKQ are always synchronized, by design, and do not require a pulse from DCLK_RST to become synchronized. The DCLK_RST signal must observe certain timing requirements, which are shown in Figure 8-6 of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{PWR}, t_{SR} and t_{HR} and may be found in AC Electrical Characteristics .

The DCLK_RST signal can be asserted asynchronously to the input clock. If

DCLK_RST is asserted, the DCLK output is held in a designated state (logic-high) in Demux Mode; in Non-Demux Mode, the DCLK continues to function normally. Depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted, there are t_{SYNC_DLY} CLK cycles of systematic delay and the next CLK rising edge synchronizes the DCLK output with those of other B12D1000RH in the system. For 90 ° Mode (DDRPh = logic-high), the synchronizing edge occurs on the rising edge of CLK, 4 cycles after the first rising edge of CLK after DCLK_RST is released. For 0 ° Mode (DDRPh = logic-low), this is 5 cycles instead. The DCLK output is enabled again after a constant delay of tOD.

For both Demux and Non-Demux Modes, there is some uncertainty about how DCLK comes out of the reset state for the first DCLK_RST pulse. For the second (and subsequent) DCLK_RST pulses, the DCLK will come out of the reset state in a known way. Therefore, if using the DCLK Reset feature, it is recommended to apply one "dummy" DCLK_RST pulse before using the second DCLK_RST pulse to synchronize the outputs. This recommendation applies each time the device or channel is powered-on.

When using DCLK_RST to synchronize multiple B12D1000RH, it is required that the Select Phase bits in the Control Register (Addr: Eh, Bits 3,4) be the same for each Master B12D1000RH.

9.5 Supply/Grounding, Layout and Thermal Recommendations

Power Planes

All supply buses for the ADC should be sourced from a common linear voltage regulator. This ensures that all power buses to the ADC are turned on and off simultaneously. This single source will be split into individual sections of the power plane, with individual decoupling and connection to the different power supply buses of the ADC. Due to the low voltage but relatively high supply current requirement, the optimal solution may be to use a switching regulator to provide an intermediate low voltage, which is then regulated down to the final ADC supply voltage by a linear regulator.

Power for the ADC should be provided through a broad plane which is located on one layer adjacent to the ground plane(s). Placing the power and ground planes on adjacent layers will provide low impedance decoupling of the ADC supplies, especially at higher frequencies. The output of a linear regulator should feed into the

power plane through a low impedance multi-via connection. The power plane should be split into individual power peninsulas near the ADC. Each peninsula should feed a particular power bus on the ADC, with decoupling for that power bus connecting the peninsula to the ground plane near each power/ground pin pair. Using this technique can be difficult on many printed circuit CAD tools. To work around this, zero ohm resistors can be used to connect the power source net to the individual nets for the different ADC power buses. As a final step, the zero ohm resistors can be removed and the plane and peninsulas can be connected manually after all other error checking is completed.

Bypass Capacitors

The general recommendation is to have one 100nF capacitor for each power/ground pin pair. The capacitors should be surface mount multi-layer ceramic chip capacitors similar to Panasonic part number ECJ-0EB1A104K.

Ground Planes

Grounding should be done using continuous full ground planes to minimize the impedance for all ground return paths, and provide the shortest possible image/return path for all signal traces.

Power System Example

See Figure 9-9. Power is provided on one plane, with the 1.9V ADC supply being split into multiple zones or peninsulas for the specific power buses of the ADC. Decoupling capacitors are connected between these power bus peninsulas and the adjacent ground planes using vias. The capacitors are located as close to the individual power/ground pin pairs of the ADC as possible. In most cases, this means the capacitors are located on the opposite side of the PCB to the ADC.

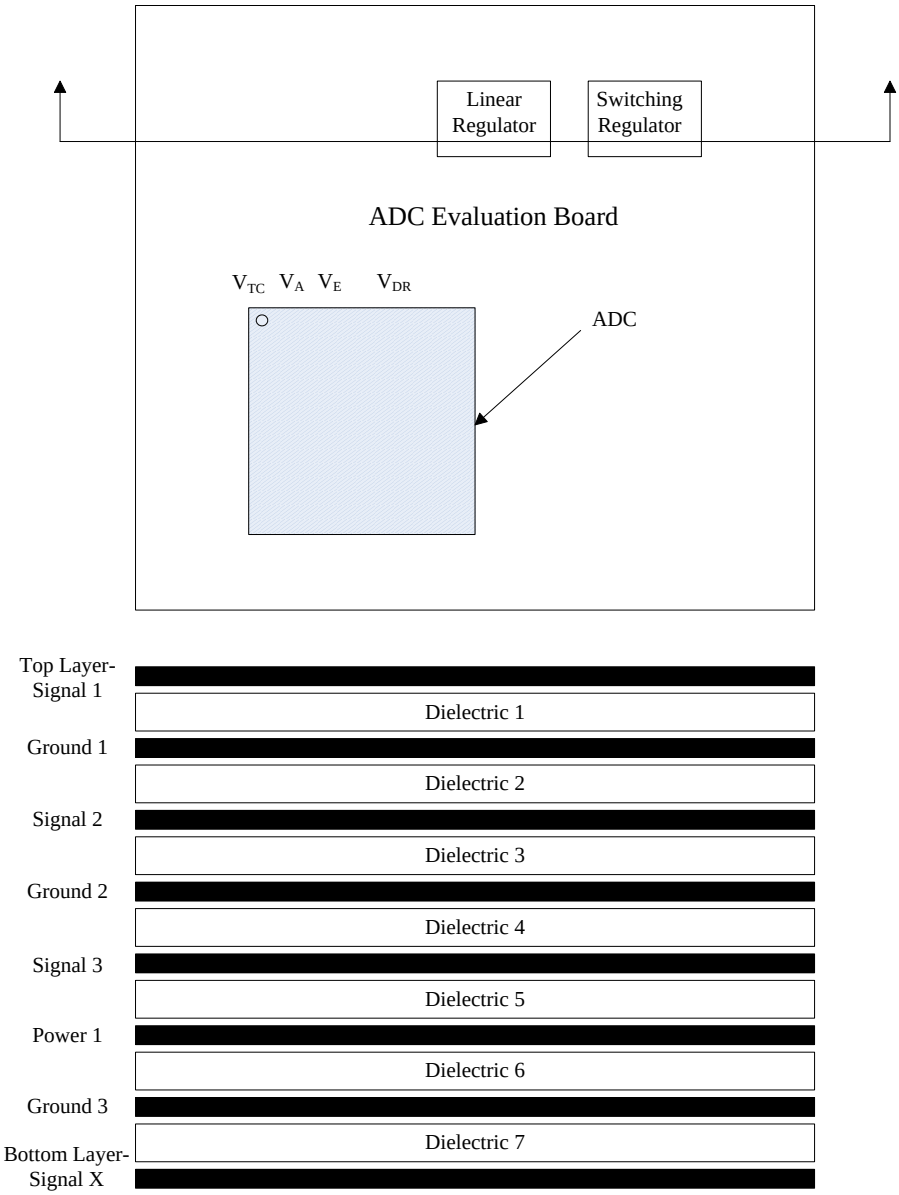


Figure 9-9. Power and Grounding Example

Thermal Management

B12D1000RH is used the Ceramic Column Grid Array (CCGA) package.

Three key parameters are provided to allow for modeling and calculations. Because there are two main thermal paths between the ADC die and external environment, the thermal resistance for each of these paths is provided. θ_{JC1} represents the thermal resistance between the die and the exposed metal area on the top of the CCGA package. θ_{JC2} represents the thermal resistance between the die and the center group of balls on the bottom of the CCGA package. The final parameter is the allowed maximum junction temperature, T_J.

In other applications, a heat sink or other thermally conductive path can be added to the top of the CCGA package to remove heat. In those cases, θ_{JC1} can be used along

with the thermal parameters for the heat sink or other thermal coupling added. In many applications, the printed circuit board will provide the primary thermal path conducting heat away from the ADC package. In those cases, θ_{JC2} can be used in conjunction with printed circuit board thermal modeling software to determine the allowed operating conditions that will maintain the die temperature below the maximum allowable limit. Additional dissipation can be achieved by coupling a heat sink to the copper pour area on the bottom side of the printed circuit board.

Typically, dissipation will occur through one predominant thermal path. In these cases, the following calculations can be used to determine the maximum safe ambient operating temperature for the B12D1000RH, for example:

$$T_J = T_A + P_D \times (\theta_{JC} + \theta_{CA})$$

$$T_J = T_A + P_{C(MAX)} \times (\theta_{JC} + \theta_{CA})$$

For θ_{JC}, the value for the primary thermal path in the given application environment should be used (θ_{JC1} or θ_{JC2}). θ_{CA} is the thermal resistance from the case to ambient, which would typically be that of the heat sink used. Using this relationship and the desired ambient temperature, the required heat sink thermal resistance can be found. Alternately, the heat sink thermal resistance can be used to find the maximum ambient temperature. For more complex systems, thermal modeling software can be used to evaluate the printed circuit board system and determine the expected junction temperature given the total system dissipation and ambient temperature.

9.6 System Power-on Considerations

There are a couple important topics to consider associated with the system power-on event including configuration and calibration, and the Data Clock.

Power-on, Configuration, and Calibration

Following the application of power to the B12D1000RH, several events must take place before the output from the B12D1000RH is valid and at full performance; at least one full calibration must be executed with the device configured in the desired mode.

Following the application of power to the B12D1000RH, there is a delay of t_{CalDly} and then the Power-on Calibration is executed. This is why it is recommended to set the CalDly Pin via an external pull-up or pull-down resistor. This ensures that the state of that input will be properly set at the same time that power is applied to the ADC and t_{CalDly} will be a known quantity. For the purpose of this section, it is

assumed that CalDly is set as recommended.

The Control Bits or Pins must be set or written to configure the B12D1000RH in the desired mode. This must take place via either Extended Control Mode or Non-ECM (Pin Control Mode) before subsequent calibrations will yield an output at full performance in that mode. Some examples of modes include DES/Non- DES Mode, Demux/Non-demux Mode, and Full-Scale Range.

The simplest case is when device is in Non-ECM and the Control Pins are set by pull-up/down resistors, see Figure 9-10. For this case, the settings to the Control Pins ramp concurrently to the ADC voltage. Following the delay of tCalDly and the calibration execution time, t_{CAL}, the output of the B12D1000RH is valid and at full performance. If it takes longer than t_{CalDly} for the system to stabilize at its operating temperature, it is recommended to execute an on-command calibration at that time.

Another case is when the FPGA configures the Control Pins (Non-ECM) or writes to the SPI (ECM), see Figure 9-11. It is always necessary to comply with the Operating Ratings and Absolute Maximum ratings, i.e. the Control Pins may not be driven below the ground or above the supply, regardless of what the voltage currently applied to the supply is. Therefore, it is not recommended to write to the Control Pins or SPI before power is applied to the B12D1000RH. As long as the FPGA has completed writing to the Control Pins or SPI, the Power-on Calibration will result in a valid output at full performance. Once again, if it takes longer than t_{CalDly} for the system to stabilize at its operating temperature, it is recommended to execute an on-command calibration at that time.

Due to system requirements, it may not be possible for the FPGA to write to the Control Pins or SPI before the Power-on Calibration takes place, see Figure 9-12. It is not critical to configure the device before the Power-on Calibration, but it is critical to realize that the output for such a case is not at its full performance. Following an On-command Calibration, the device will be at its full performance.

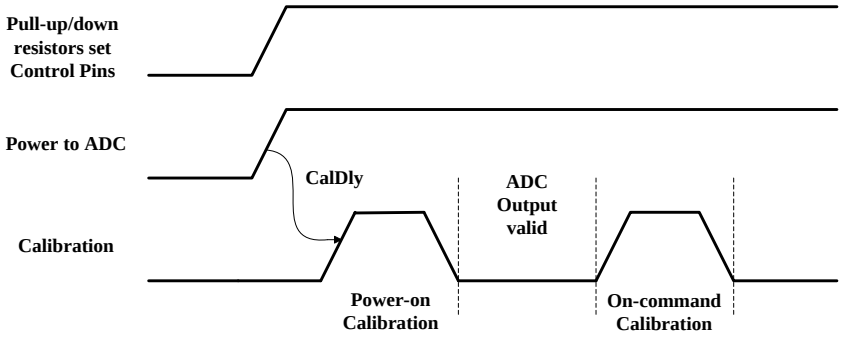


Figure 9-10. Power-on with Control Pins set by Pull-up/down Resistors

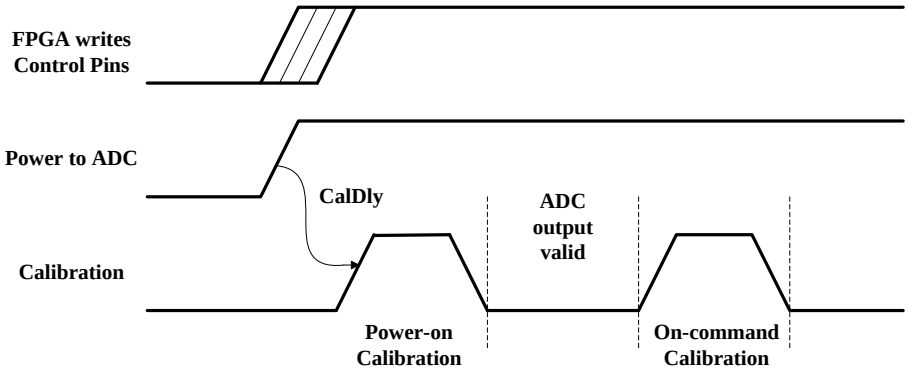


Figure 9-11. Power-on with Control Pins set by FPGA pre Power-on Cal

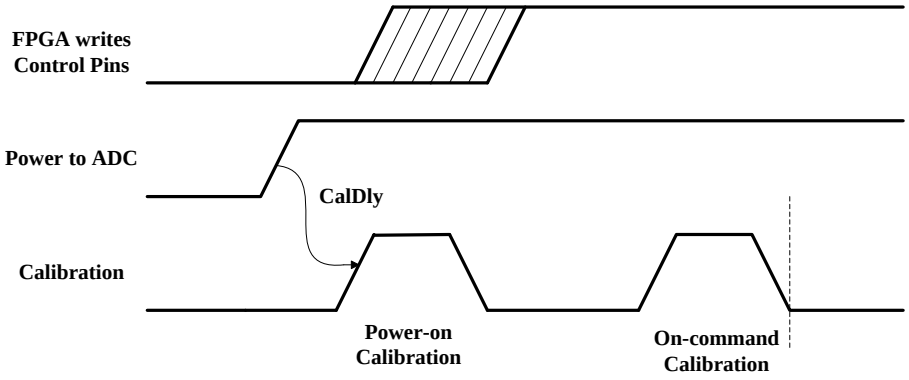


Figure 9-12. Power-on with Control Pins set by FPGA post Power-on Cal

Power-on and Data Clock (DCLK)

Many applications use the DCLK output for a system clock. For the B12D1000RH, each I- and Q-channel has its own DCLKI and DCLKQ, respectively. The DCLK output is always active, unless that channel is powereddown or the DCLK Reset feature is used while the device is in Demux Mode. As the supply to the B12D1000RH ramps, the DCLK also comes up, see Figure 9-13. While the supply is too low, there is no output at DCLK. As the supply continues to ramp, DCLK functions intermittently with irregular frequency, but the amplitude continues to track with the supply. Much below the low end of operating supply range of the B12D1000RH, the DCLK is already fully operational.

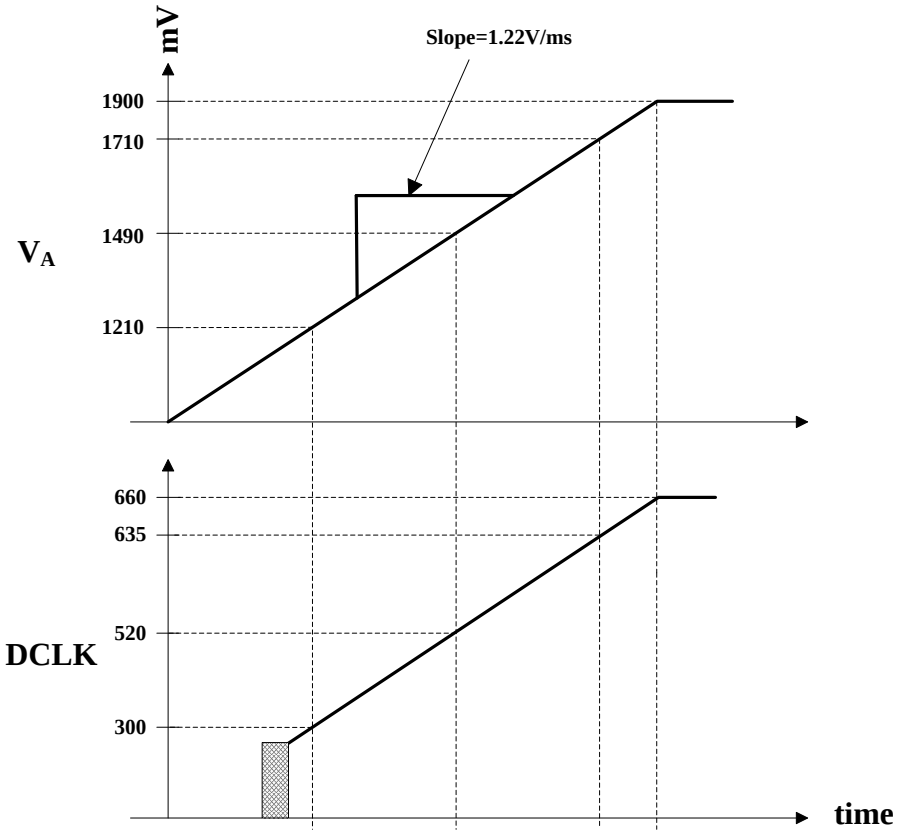


Figure 9-13. Supply and DCLK Ramping

RECOMMENDED SYSTEM CHIPS

Recommends these other chips including temperature sensors, clocking devices, and amplifiers in order to support the B12D1000RH in a system design.

Temperature Sensor

The B12D1000RH has an on-die temperature diode connected to pins Tdiode+/- which may be used to monitor the die temperature. TI also provides a family of temperature sensors for this application which monitor different numbers of external devices, see Table 9-12.

Table 9-12 Temperature Sensor Recommendation

Number of External Devices Monitored	Recommended Temperature Sensor
1	LM95235
2	LM95213
4	LM95214

The temperature sensor (LM95235/13/14) is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface that can monitor the temperature of one, two, or four remote diodes as well as its own temperature. It can be used to accurately monitor the temperature of up to one, two, or four external devices such as the B12D1000RH, a FPGA, other system components, and the

ambient temperature.

Diode fault detection circuitry in the temperature sensor can detect the absence or fault state of a remote diode: whether D+ is shorted to the power supply, D- or ground, or floating. In the following typical application, the LM95213 is used to monitor the temperature of an B12D1000RH as well as an FPGA, see Figure 9-14. If this feature is unused, the Tdiode+/- pins may be left floating.

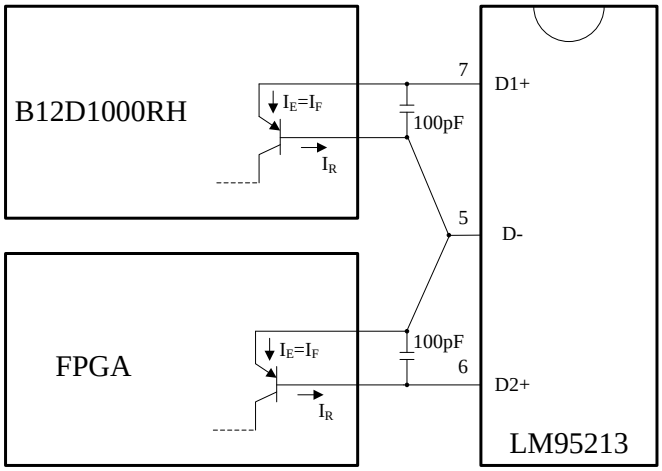


Figure 9-14. Typical Temperature Sensor Application

Clocking Device

The clock source can be a PLL/VCO device such as the LMX2531LQxxxx family of products. The specific device should be selected according to the desired ADC sampling clock frequency. Devices which may be considered based on clock source, jitter cleaning, and distribution purposes are the LMK01XXX, LMK02XXX, LMK03XXX and LMK04XXX product families.

Amplifiers for the Analog Input

The following amplifiers can be used for B12D1000RH applications which require DC coupled input or signal gain, neither of which can be provided with a transformer coupled input circuit:

Table 9-13 Amplifier Recommendations

Amplifier	Bandwidth	Brief features
LMH6552	1.5GHz	Configurable gain
LMH6553	900MHz	Output clamp and configurable gain
LMH6554	2.8GHz	Configurable gain
LMH6555	1.2GHz	Fixed gain

Balun Recommendations for Analog Input

The following baluns are recommended for the B12D1000RH for applications which require no gain. When evaluating a balun for the application of driving an ADC,

some important qualities to consider are phase error and magnitude error.

Table 9-14 Balun Recommendations

Balun	Bandwidth
Mini Circuits TC1-1-13MA+	4.5 – 3000MHz
Anaren B0430J50100A00	400 – 3000MHz
Mini Circuits ADTL2-18	30 – 1800MHz

9.7 Register Definitions

Ten read/write registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Non-extended Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit. See Table 9-15 for a summary. For a description of the functionality and timing to read/write the control registers, see The Serial Interface.

Table 9-15 Register Addresses

A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Configuration Register
0	0	0	1	1h	Reserved
0	0	1	0	2h	I-channel Offset
0	0	1	1	3h	I-channel Full-Scale Range
0	1	0	0	4h	Calibration Adjust
0	1	0	1	5h	Calibration Values
0	1	1	0	6h	Reserved
0	1	1	1	7h	DES Timing Adjust
1	0	0	0	8h	Reserved
1	0	0	1	9h	Reserved
1	0	1	0	Ah	Q-channel Offset
1	0	1	1	Bh	Q-channel Full-Scale Range
1	1	0	0	Ch	Aperture Delay Coarse Adjust
1	1	0	1	Dh	Aperture Delay Fine Adjust
1	1	1	0	Eh	AutoSync
1	1	1	1	Fh	Reserved

Table 9-16 Configuration Register

Addr:0h(0000b)									POR:2000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	LFS	DES	DEQ	DIQ	2SC	TSE	Res		
POR	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	CAL: Calibration Enable. When this bit is set to 1b, an on-command calibration is initiated. This bit is not reset automatically upon completion of the calibration.

	Therefore, the user must reset this bit to 0b and then set it to 1b again to execute another calibration. This bit is logically OR'd with the CAL Pin; both bit and pin must be set to 0b before either is used to execute a calibration.
Bit 14	DPS: DCLK Phase Select. In DDR, set this bit to 0b to select the 0 °Mode DDR Data-to-DCLK phase relationship and to 1b to select the 90 °Mode. If the device is in Non-Demux Mode, this bit has no effect; the device will always be in 0 ℃DR Mode.
Bit 13	OVS: Output Voltage Select. This bit sets the differential voltage level for the LVDS outputs including Data, OR, and DCLK. 0b selects the lower level and 1b selects the higher level. See V_{OD} in Digital Control and Output Pin Characteristics for details.
Bit 12	TPM: Test Pattern Mode. When this bit is set to 1b, the device will continually output a fixed digital pattern at the digital Data and OR outputs. When set to 0b, the device will continually output the converted signal, which was present at the analog inputs. See Test Pattern Mode for details about the TPM pattern.
Bit 11	PDI: Power-down I-channel. When this bit is set to 0b, the I-channel is fully operational; when it is set to 1b, the I-channel is powered-down. The I-channel may be powered-down via this bit or the PDI Pin, which is active, even in ECM.
Bit 10	PDQ: Power-down Q-channel. When this bit is set to 0b, the Q-channel is fully operational; when it is set to 1b, the Q-channel is powered-down. The Q-channel may be powered-down via this bit or the PDQ Pin, which is active, even in ECM.
Bit 9	Reserved. Must be set to 0b.
Bit 8	LFS: Low-Frequency Select. If the sampling clock (CLK) is at or below 300 MHz, set this bit to 1b for improved performance.
Bit 7	DES: Dual-Edge Sampling Mode select. When this bit is set to 0b, the device will operate in the Non-DES Mode; when it is set to 1b, the device will operate in the DES Mode. See DES/Non-DES Mode for more information.
Bit 6	DEQ: DES Q-input select, a.k.a. DESQ Mode. When the device is in DES Mode, this bit selects the input that the device will operate on. The default setting of 0b selects the I-input and 1b selects the Q-input.
Bit 5	DIQ: DES I- and Q-input, a.k.a. DESIQ Mode. When in DES Mode, setting this bit to 1b shorts the I- and Q-inputs internally to the device. If the bit is left at its default 0b, the I- and Q-inputs remain electrically separate. To operate the device in DESIQ Mode, Bits<7:5> must be set to 101b. In this mode, both the I- and Q-inputs must be externally driven; see DES/Non-DES Mode for more information.
Bit 4	2SC: Two's Complement output. For the default setting of 0b, the data is output in Offset Binary format; when set to 1b, the data is output in Two's Complement format.
Bit 3	TSE: Time Stamp Enable. For the default setting of 0b, the Time Stamp feature is not enabled; when set to 1b, the feature is enabled. See Output Control and Adjust for more information about this feature.
Bits 2:0	Reserved. Must be set as shown.

Table 9-17 Reserved

Addr:1h(0001b)									POR:2A0Eh							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	Res															
POR	0	0	1	0	1	0	1	0	0	0	0	0	1	1	1	0

Bits 15:0	Reserved. Must be set as shown.

Table 9-18 I-channel Offset Adjust

Addr:2h(0010b)									POR:0000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM（11:0）											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13	Reserved. Must be set to 0b.	
Bit 12	OS: Offset Sign. The default setting of 0b incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1b incurs a negative offset of the set magnitude.	
Bits 11:0	OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0d to 45 mV for OM(11:0) = 4095d in steps of ~11 µV. Monotonicity is ensured by design only for the 9 MSBs.	
	Code	**Offset（mV）**
	0000 0000 0000（default）	0
	1000 0000 0000	22.5
	1111 1111 1111	45

Table 9-19 I-channel Full Scale Range Adjust

Addr:3h(0011b)									POR:4000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM（14:0）														
POR	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	Reserved. Must be set to 0b.	
Bits 14:0	FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0d) to 1000 mV (32767d) with the default setting at 800 mV (16384d). Monotonicity is ensured by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, i.e. FSR values above 800 mV. See VIN_FSR in Analog Input/Output and Reference Characteristics for characterization details.	
	Code	**FSR（mV）**
	000 0000 0000 0000	600
	100 0000 0000 0000（default）	800
	111 1111 1111 1111	1000

Table 9-20 Calibration Adjust

Addr:4h(0100b)																POR:DF4Bh
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	CSS	Res						SSC	Res						
POR	1	1	0	1	1	1	1	1	0	1	0	0	1	0	1	1

Bit 15	Reserved. Must be set as shown
Bit 14	CSS: Calibration Sequence Select. The default 1b selects the following calibration sequence: reset all previously calibrated elements to nominal values, do R_{IN} Calibration, do internal linearity Calibration. Setting CSS = 0b selects the following calibration sequence: do not reset RIN to its nominal value, skip R_{IN} calibration, do internal linearity Calibration. The calibration must be completed at least one time with CSS = 1b to calibrate R_{IN}. Subsequent calibrations may be run with CSS = 0b (skip R_{IN} calibration) or 1b (full R_{IN} and internal linearity Calibration).
Bit 13:8	Reserved. Must be set as shown.
Bit 7	SSC: SPI Scan Control. Setting this control bit to 1b allows the calibration values, stored in Addr: 5h, to be read/written. When not reading/writing the calibration values, this control bit should left at its default 0b setting. See Calibration Feature for more information.
Bit 6:0	Reserved. Must be set as shown.

Table 9-21 Calibration Values

Addr:5h(0101b)																POR:XXXXh
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SS（15:0）															
POR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit 15:0	SS(15:0): SPI Scan. When the ADC performs a self-calibration, the values for the calibration are stored in this register and may be read from/ written to it. Set SSC (Addr: 4h, Bit 7) to read/write. See Calibration Feature for more information.

Table 9-22 Reserved

Addr:6h(0110b)																POR:1C20h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0

Bits 15:0	Reserved. Must be set as shown.

Table 9-23 DES Timing Adjust

Addr:7h(0111b)																POR:8140h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTA（6:0）							Res								

POR	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

Bit 15:9	DTA(6:0): DES Mode Timing Adjust. In the DES Mode, the time at which the falling edge sampling clock samples relative to the rising edge of the sampling clock may be adjusted; the automatic duty cycle correction continues to function. See Input Control and Adjust for more information. The nominal step size is 30fs.
Bit 8:0	Reserved. Must be set as shown.

Table 9-24 Reserved

Addr:8h(1000b)									POR:0000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0	Reserved. Must be set as shown.

Table 9-25 Reserved

Addr:9h(1001b)									POR:0000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0	Reserved. Must be set as shown.

Table 9-26 Q-channel Offset Adjust

Addr:Ah(1010b)									POR:0000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM（11:0）											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13	Reserved. Must be set to 0b.	
Bit 12	OS: Offset Sign. The default setting of 0b incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1b incurs a negative offset of the set magnitude.	
Bits 11:0	OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0d to 45 mV for OM(11:0) = 4095d in steps of ~11 μV. Monotonicity is ensured by design only for the 9 MSBs.	
	Code	**Offset（mV）**
	0000 0000 0000（default）	0
	1000 0000 0000	22.5
	1111 1111 1111	45

Table 9-27 Q-channel Full-Scale Range Adjust

Addr:Bh(1011b)									POR:4000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM（14:0）														
POR	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	Reserved. Must be set to 0b.	
Bits 14:0	FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0d) to 1000 mV (32767d) with the default setting at 800 mV (16384d). Monotonicity is ensured by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, i.e. FSR values above 800 mV. See V_{IN_FSR} in Analog Input/Output and Reference Characteristics for characterization details.	
	Code	**FSR（mV）**
	000 0000 0000 0000	600
	100 0000 0000 0000（default）	800
	111 1111 1111 1111	1000

Table 9-28 Aperture Delay Coarse Adjust

Addr:Ch(1100b)									POR:0004h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM（11:0）												STA	DCC	Res	
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit 15:4	CAM(11:0): Coarse Adjust Magnitude. This 12-bit value determines the amount of delay that will be applied to the input CLK signal. The range is 0 ps delay for CAM(11:0) = 0d to a maximum delay of 825 ps for CAM(11:0) = 2431d (±95 ps due to PVT variation) in steps of ~340 fs. For code CAM(11:0) = 2432d and above, the delay saturates and the maximum delay applies. Additional, finer delay steps are available in register Dh. The STA (Bit 3) must be selected to enable this function.
Bit 3	STA: Select tAD Adjust. Set this bit to 1b to enable the tAD adjust feature, which will make both coarse and fine adjustmentsettings, i.e. CAM(11:0) and FAM(5:0), available.
Bit 2	DCC: Duty Cycle Correct. This bit can be set to 0b to disable the automatic duty-cycle stabilizer feature of the chip. This feature is enabled by default.
Bit 1:0	Reserved. Must be set to 0b.

Table 9-29 Aperture Delay Fine Adjust

Addr:Dh(1101b)									POR:0000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FAM（5:0）						Res									
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:10	FAM(5:0): Fine Aperture Adjust Magnitude. This 6-bit value determines the amount of additional delay that will be applied to the input CLK when the Clock Phase Adjust feature is enabled via STA (Addr: Ch, Bit 3). The range is straight binary from 0 ps delay for FAM(5:0) = 0d to 2.3 ps delay for FAM(5:0) = 63d (±300 fs due to PVT variation) in steps of ~36 fs.
Bit 9:0	Reserved. Must be set as shown.

Table 9-30 AutoSync

Addr:Eh(1110b)															POR:0003h	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRC（8:0）								Res			SP（1:0）		ES	DOC	DR
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit 15:7	DRC(8:0): Delay Reference Clock (8:0). These bits may be used to increase the delay on the input reference clock when synchronizing multiple ADCs. The delay may be set from a minimum of 0s (0d) to a maximum of 1000 ps (319d). The delay remains the maximum of 1000 ps for any codes above or equal to 319d. See SYNCHRONIZING MULTIPLE B12D1000RH IN A SYSTEM for more information.
Bit 6:5	Reserved. Must be set as shown.
Bit 4:3	SP（1:0）：Select Phase. These bits select the phase of the reference clock which is latched. The codes correspond to the following phase shift: 00 = 0 ° 01 = 90 ° 10 = 180 ° 11 = 270 °
Bit 2	ES: Enable Slave. Set this bit to 1b to enable the Slave Mode of operation. In this mode, the internal divided clocks are synchronized with the reference clock coming from the master ADC. The master clock is applied on the input pins RCLK. If this bit is set to 0b, then the device is in Master Mode.
Bit 1	DOC: Disable Output reference Clocks. Setting this bit to 0b sends a CLK/4 signal on RCOut1 and RCOut2. The default setting of 1b disables these output drivers. This bit functions as described, regardless of whether the device is operating in Master or Slave Mode, as determined by ES (Bit 2).
Bit 0	DR: Disable Reset. The default setting of 1b leaves the DCLK_RST functionality disabled. Set this bit to 0b to enable DCLK_RST functionality.

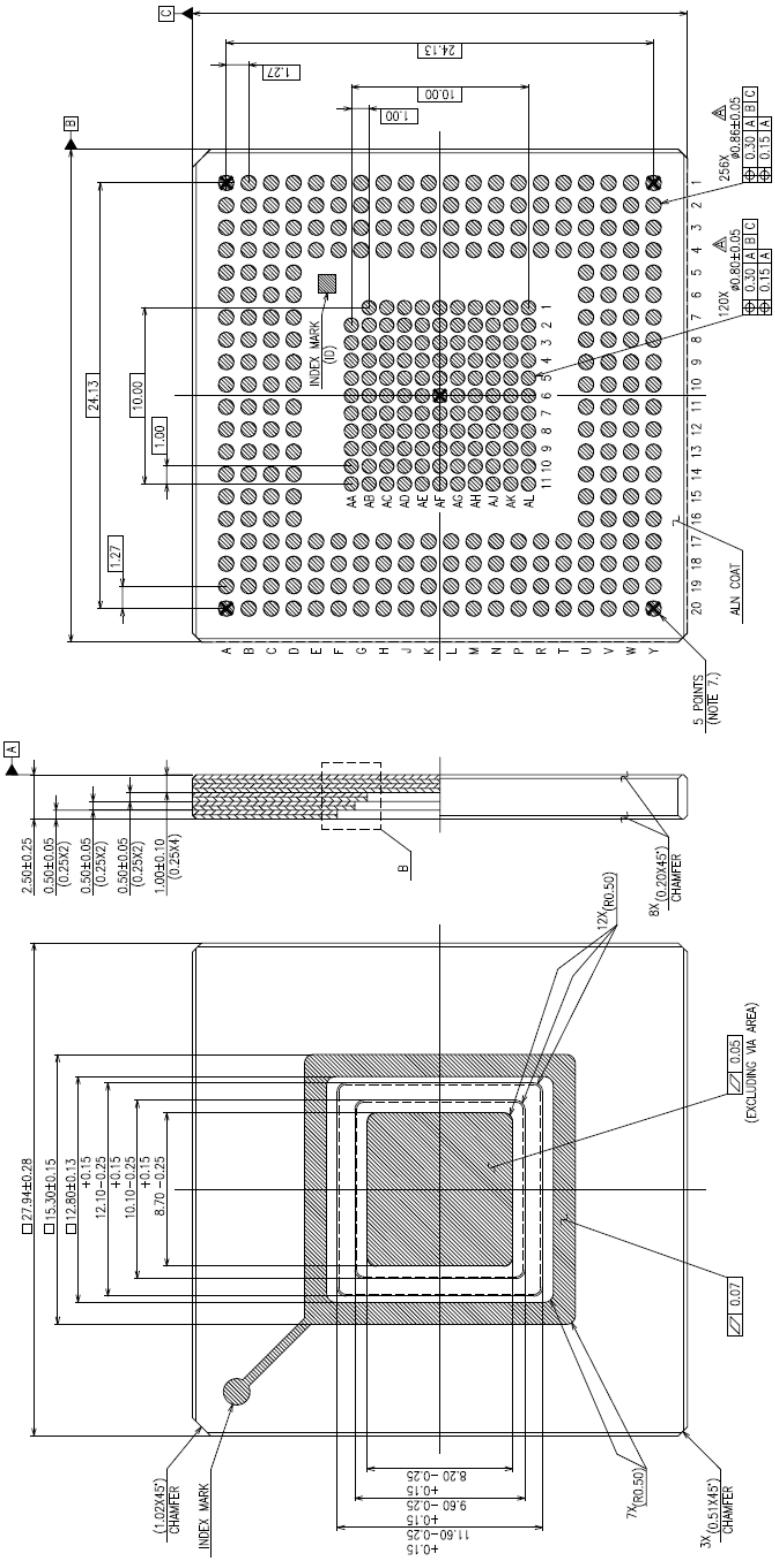
Table 9-31 Reserved

Addr:Fh(1111b)															POR:0018h	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bits 15:0	Reserved. Must be set as shown.

10. Package Outline Dimension

B12D1000RH dimentions are in millimeters



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