Ver 1.1

10-bit 500K analog to digital converter

Datasheet

Part Number：B7892RH

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Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.01		Initial release.	
1.1	2018.03		Update format	

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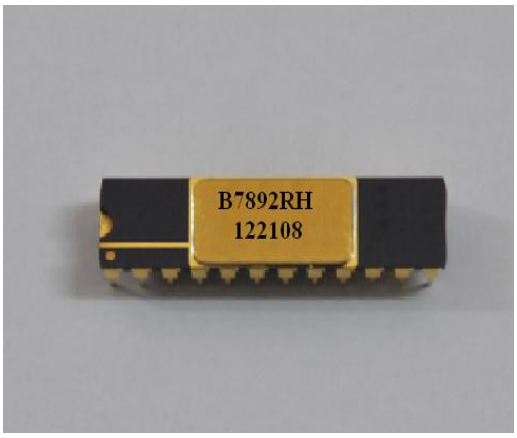
1. Features

- **Electrical characteristics**
  - Fast 12-Bit ADC with 1.68 us Conversion Time
  - 500 kSPS Throughput Rate
  - Single Supply Operation
  - On-Chip Track/Hold Amplifier
  - Selection of Input Ranges: ±10 V or ±5 V
  - High Speed Serial and Parallel Interface
  - Low Power, 110 mW typ
  - Overvoltage Protection on Analog Inputs
- **Reliability features**
  - Operating temperature ：-55℃ ～ +125℃
  - ESD feature （human body model）：2000V
  - Electrical latch up feature：200mA
  - Total ionizing dose：≥100Krad（Si）
  - Single event latch-up threshold：≥75MeV·cm^2/mg



2. General Description

The B7892RH is a high speed, low power, 12-bit A/D converter that operates from a single +5 V supply. The part contains a1.68 us successive approximation ADC, an on-chip track/hold amplifier, an internal +2.5 V reference and on-chip versatile interface structures that allow both serial and parallel connection to a microprocessor. The part accepts an analog input range of ±10 V or ±5 V. Overvoltage protection on the analog inputs for the B7892RH allows the input voltage to go to ±17 V or ±7 V respectively without damaging the ports.

The B7892RH offers a choice of two data output formats: a single, parallel, 12-bit word or serial data. Fast bus access times and standard control inputs ensure easy parallel interface to microprocessors and digital signal processors. A high speed serial interface allows direct connection to the serial ports of microcontrollers and digital signal processors.

3. Function Block Diagram

B7982RH function block diagram is shown in figure 3-1.

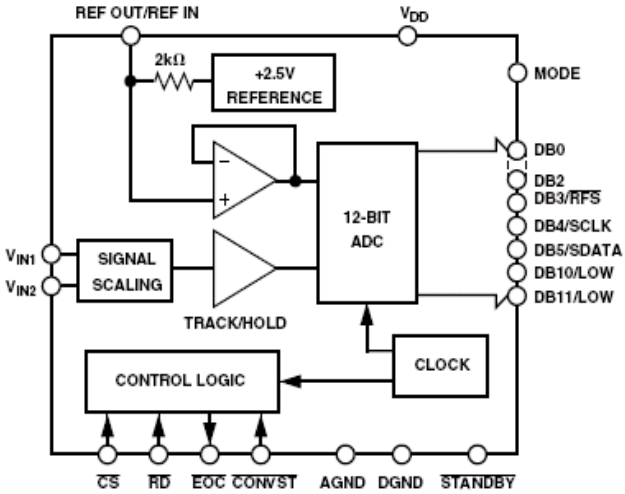


Figure 3-1 function block digram

4. Packages and Pin Function Descriptions

The B7892RH is packaged in a leaded CDIP24 package, the work temperature range is -55℃ to +125℃.

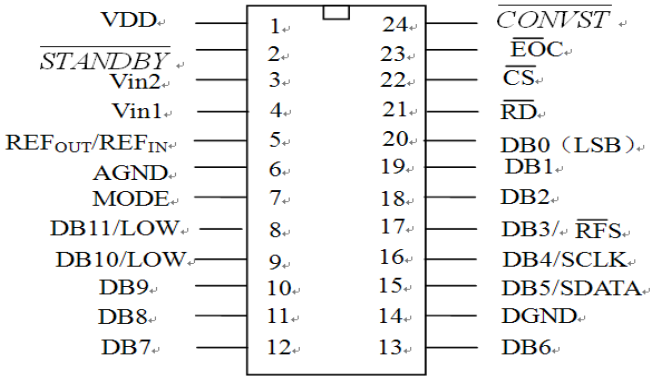


Figure 4-1 Connetion pin diagram(Top View)

Table 4-1 Pin Function Descriptions

1	VDD	Positive Supply Voltage, +5 V ±5%.
2	$\overline{STANDBY}$	Standby Input. Logic Input. With this input at a logic high, the part is in its normal operating mode; with this input at a logic low, the part is placed in its standby or power-down mode, which reduces power consumption to 5 mW typical.
3	VIN2	Analog Input 2. this input either connects to AGND or to VIN1 to determine the analog input voltage range. With VIN2 connected to AGND , the analog input range at the VIN1 input is ±10 V. With VIN2 connected to VIN1, the analog input range to the part is ±5 V.
4	VIN1	the input voltage range is either ±5 V or ±10 V depending on where the VIN2 input is connected.
5	REF	Voltage Reference Output/Input. The part can be used with either its own internal reference or with an external reference source. The on-chip +2.5 V reference is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should be decoupled to AGND with a 0.1 μF disc ceramic capacitor. The output impedance of this reference source is typically 5.5 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The REF IN input is buffered on-chip but must be able to sink or source current through the resistor to the output of the on-chip reference.
6	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
7	MODE	With this pin at a logic low, the device is in its serial interface mode; with this pin at a logic high, the device is in its parallel interface mode.
8	DB11	Data Bit 11/Test Pin. When the device is in its parallel mode, this pin is Data Bit 11 (MSB), a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation.
9	DB10	Data Bit 10/Test Pin. When the device is in its parallel mode, this pin is Data Bit 10, a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation .
10	DB9	Data Bit 9.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.

14	DGND	Digital Ground. Ground reference for digital circuitry.
15	DB5	Data Bit 5/Serial Data. When the device is in its parallel mode, this pin is Data Bit 5, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial data output line. Sixteen bits of serial data are provided with four leading zeros preceding the 12 bits of valid data. Serial data is valid on the falling edge of SCLK for sixteen edges after *RFS* goes low. Output coding is two's complement.
16	DB4	Data Bit 4/Serial Clock. When the device is in its parallel mode, this pin is Data Bit 4, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial clock pin, SCLK. SCLK is an input and an external serial clock must be provided at this pin to obtain serial data from the B7892RH. Serial data is clocked out from the output shift register on the rising edges of SCLK after *RFS* goes low.
17	DB3	Data Bit 3/Receive Frame Synchronization. When the device is in its parallel mode, this pin is Data Bit 3, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the receive frame synchronization input with *RFS* provided externally to obtain serial data .
18	DB2	Data Bit 2
19	DB1	Data Bit 1
20	DB0	Data Bit 0
21	$\overline{RD}$	Read. Active low logic input which is used in conjunction with *CS* low to enable the data outputs.
22	$\overline{CS}$	Chip Select. Active low logic input which is used in conjunction with *RD* to enable the data outputs.
23	$\overline{EOC}$	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low going pulse on this line. The duration of this *EOC* pulse is nominally 100 ns.
24	$\overline{CONVST}$	Convert Start. Logic Input. A low-to-high transition on this input puts the track/hold into its hold mode and starts conversion.

5. Electrical Characteristics

5.1 DC Electrical Characteristics

Table 5-1 DC Parameter Table

Parameter	Symbol	Condition	Limits		UNIT
		（VDD=5×(1±5%) V, -55℃≤ T_A ≤ 125℃）	MIN	MAX	
Logic Input					
High-level input voltage	V_{IH}		2.4	—	V
Low-level input voltage	V_{IL}		—	0.8	V
High-level input current	I_{IH}	$V_I=V_{DD}$	-10.0	10.0	μA
Low-level input current	$/I_{IL}/$	V_I=0V		10.0	μA
Logic Output					
High-level output voltage	V_{OH}	CMOS：I_{OH}=-200 uA	4	—	V
Low-level output voltage	V_{OL}	CMOS：I_{OL}= 1.6mA	—	0.4	V
Power Requirement					
Supply voltage	V_{DD}		4.5	5.5	V
Supply current	I_{DD}	Operating mode	—	22	mA
Reference voltage					
Reference voltage	*ref*		2.475	2.525	V
DC Accuracy					
Resolution			10	—	Bits
Differential Non-Linearity	*DNL*		-1	1	LSB
Integral Non-Linearity	*INL*		-1	1	LSB

5.2 AC Electrical Characteristics

Table 5-2 AC Parameter Table

Parameter	Symbol	Condition	Limits		UNIT
		（VDD =5×(1±5%)V,-55℃ ≤ T_A≤ 125℃）	MIN	MAX	
Signal to noise and distortion	*SINAD*		54	—	dB
Total harmonic distortion	*THD*		—	-65	dB
Spurious free dynamic rang	*SFDR*		65	—	dB
Conversion time[a]	t_{CONV}		—	1.68	μs

5.3 Absolute Maximum Ratings

Table 5-3 Absolute Maximum Ratings

Parameter	Symbol	Value	UNIT
VDD	VDD	-0.3 to 7	V
Power	P_D	450	mW
Operating Temperature Range	T_A	-55~125	℃
Storage temperature range	T_{stg}	-65~150	℃
Junction temperature	T_J	175	℃

6. Detailed Description

6.1 Analog Input Section

The analog input range is pin-strappable (using VIN2) for either ±5 V or ±10 V on the VIN1 input. With VIN2 connected to AGND, the input range on VIN1 is ±10 V, and the input resistance on VIN1 is 15 kΩ nominal. With VIN2 connected to VIN1, the input range on VIN1 is ±5 V, and the input resistance on VIN1 is 8 kΩ nominal. As a result, the VIN1 and VIN2 inputs should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to ±17 V without damaging the B7892RH.

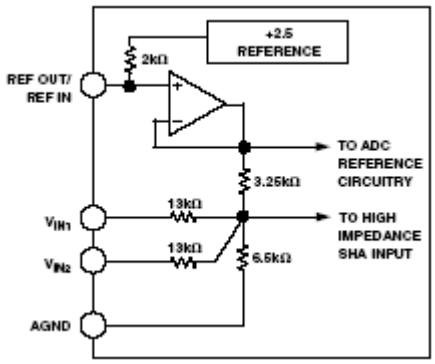


Figure6-1 Analog Input Structure

6.2 INTERFACING

The part provides two interface options, a 12-bit parallel interface and a three-wire serial interface. The required interface mode is selected via the MODE pin. The two interface modes are discussed in the following sections.

Parallel Interface Mode

The parallel interface mode is selected by tying the MODE input to a logic high. Figure 6-2 shows a timing diagram illustrating the operational sequence of the B7892RH. The on-chip track/hold goes into hold mode, and conversion is initiated on the rising edge of the CONVST signal. When conversion is complete, the end of conversion line (EOC) pulses low to indicate that new data is available in the B7892RH's output register.

This EOC line can be used to drive an edge-triggered interrupt of a microprocessor. The falling edge of the RD signal should occur 200 ns prior to the next rising edge of CONVST. CS and RD going low accesses the 12-bit conversion result. In systems where the part is interfaced to a gate array or ASIC, this EOC pulse can be applied to the CS and RD inputs to latch data out of the B7892RH and into the gate array or ASIC. This eliminates the logic required in the gate array or ASIC to recognize the end of conversion and generate the read signal for the B7892RH. To obtain optimum performance from the B7892RH, it is not recommended to tie CS and RD permanently low as this keeps the three-state active during conversion.

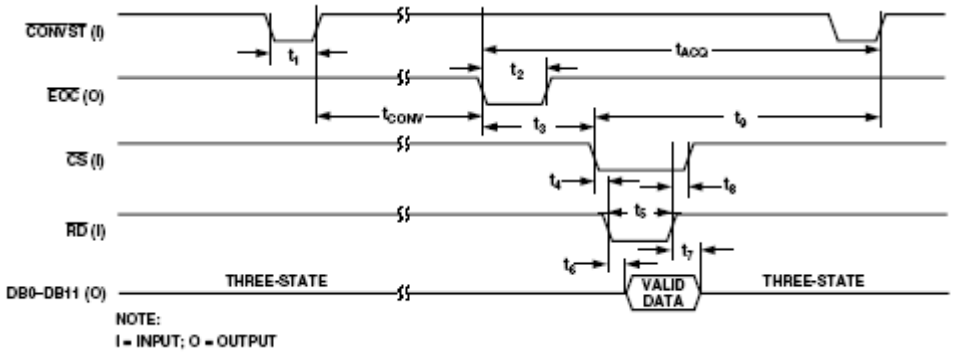


Figure6-2 Parallel Mode Timing Diagram

Serial Interface Mode

The B7892RH is configured for serial mode interfacing by tying the MODE input low. It provides for a three-wire, serial link between the B7892RH and industry-standard microprocessors, microcontrollers and digital signal processors. SCLK and RFS of the B7892RH are inputs, and the B7892RH's serial interface is designed for direct interface to systems that provide a serial clock input that is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Figure6- 3 shows the timing diagram for reading from the B7892RH in the serial interface mode. RFS goes low to access data from the B7892RH. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, RFS must remain low for the duration of the data transfer operation. Sixteen bits of data are transmitted with four leading zeros followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK. Old data is guaranteed to be valid for 5 ns after this edge. This is useful for high speed serial clocks where the access time of the part would not allow sufficient set-up time for the data to be accepted on the falling edge of the clock. In this case, care must be taken that RFS does not go just prior to a rising edge of SCLK. For slower serial clocks data is valid on the falling edge of SCLK. At the end of the read operation, the SDATA line is three-stated by a rising edge on either the SCLK or RFS inputs, whichever occurs first. Serial data cannot be read during conversion to avoid feedthrough problems from the serial clock to the conversion process. For optimum performance of the B7892RH, a serial read should also be avoided within 400 ns of the rising edge of CONVST to avoid feedthrough into the track/hold during its acquisition time. The serial read should, therefore, occur between the end of conversion (EOC falling edge) and 400 ns prior to the next rising edge of CONVST.

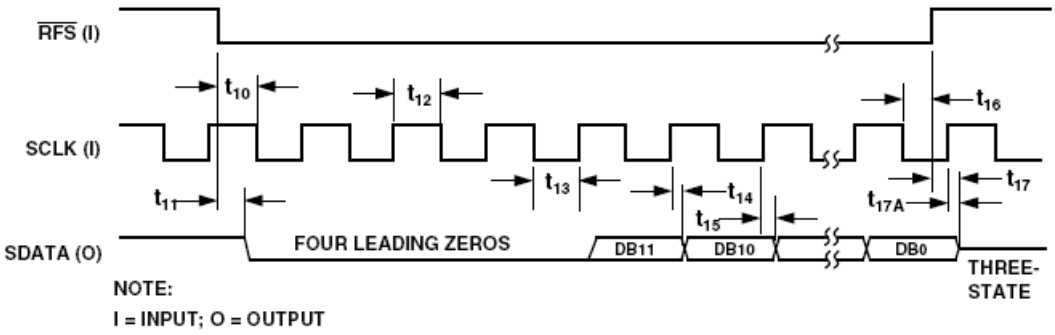


Figure6-3 Serial Mode Timing Diagram

6.3 MICROPROCESSOR INTERFACING

The B7892RH features both high speed parallel and serial interfaces, allowing considerable flexibility in interfacing to microprocessor systems. To obtain optimum performance from the part, data should not be read during conversion and this limits the achievable throughput rate in serial mode .

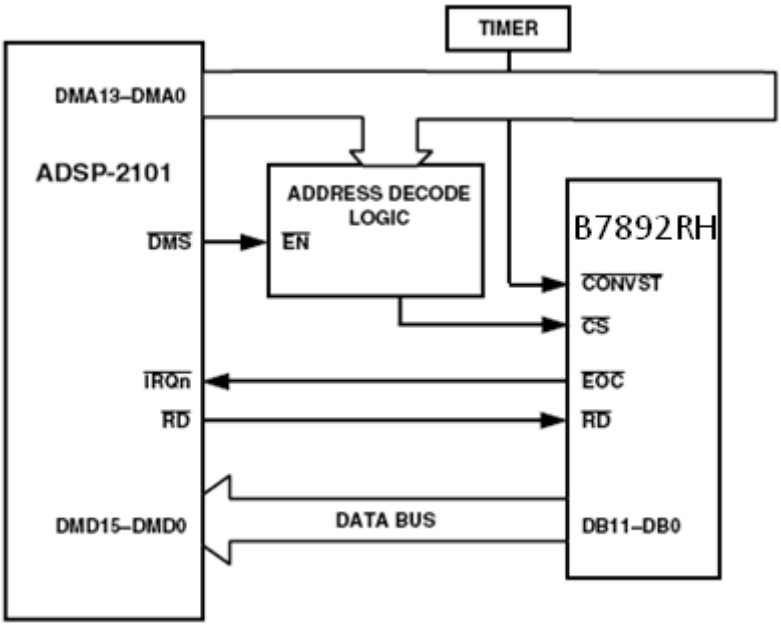


Figure6-4 B7892RH to ADSP-2101

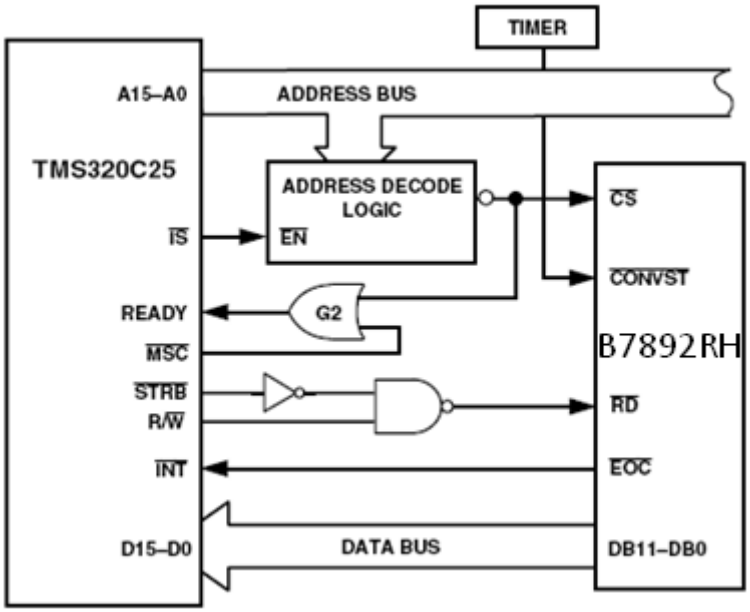


Figure 6-5 B7892RH to TMS320C25

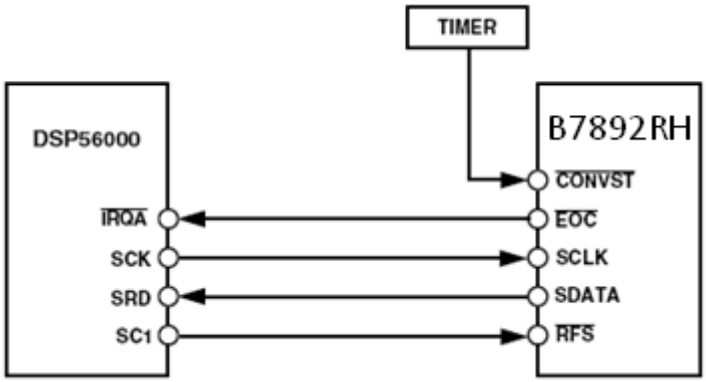


Figure6-6 B7892RH to DSP56000

7. Package Specifications

The specifications of CDIP24 package are shown in figure7-1.

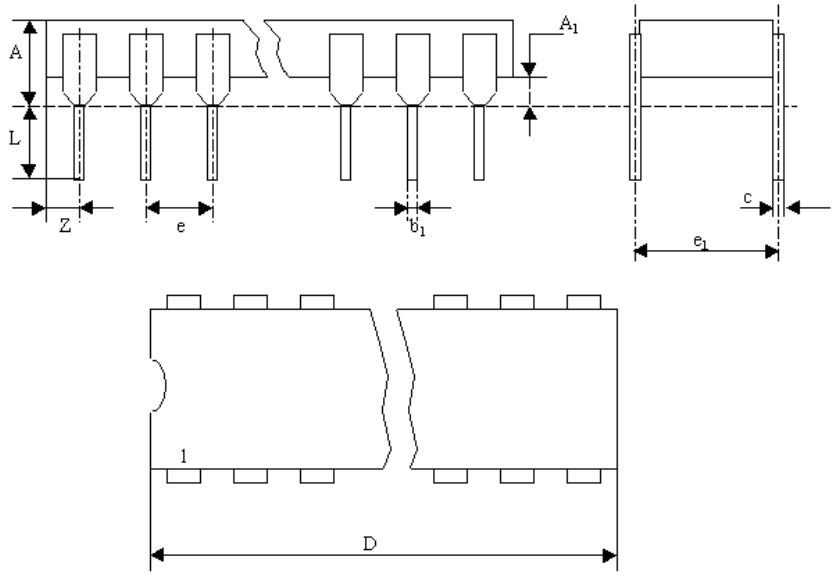


Figure 7-1 CDIP24 package specifications

Table 7-1 size symbol list

Symbol;	Value（mm）		
	MIN	Normal	MAX
D	30.18	——	30.78
e1	——	7.62	——
e	——	2.54	——
c	0.23	——	0.30
Z	——	——	1.27
A	3.09	——	3.78
A1	1.02	——	1.52
b1	0.41	——	0.51
L	——	——	4.45

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