Ver 1.1

8-Bit 3GSPS Analog to Digital Converter

Datasheet

Part Number：B083000RQC

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Page of Revise Control

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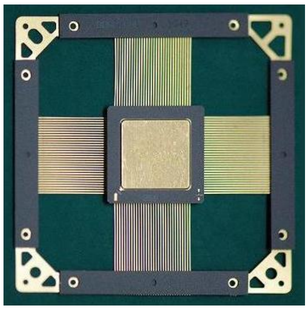
1 Unique features



- Internal Sample-and-Hold
- Single +1.9V ±0.1V Operation
- Choice of SDR or DDR output clocking
- Multiple ADC Synchronization Capability
- Guaranteed No Missing Codes
- Fine Adjustment of Input Full-Scale Range and Offset
- Serial Interface for Extended Control
- On-chip high speed digital calibration
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV cm^2/mg

2 General Description

The B083000RQC is a radiation hardened, dual, low power, high performance, CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 3.0 GSPS. Consuming a typical 1.9 Watts at 3GSPS from a single 1.9 Volt supply. The innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic performance. B083000RQC has Extended Control Mode enable user change the operational parameters for high performance.

3 Block Diagram

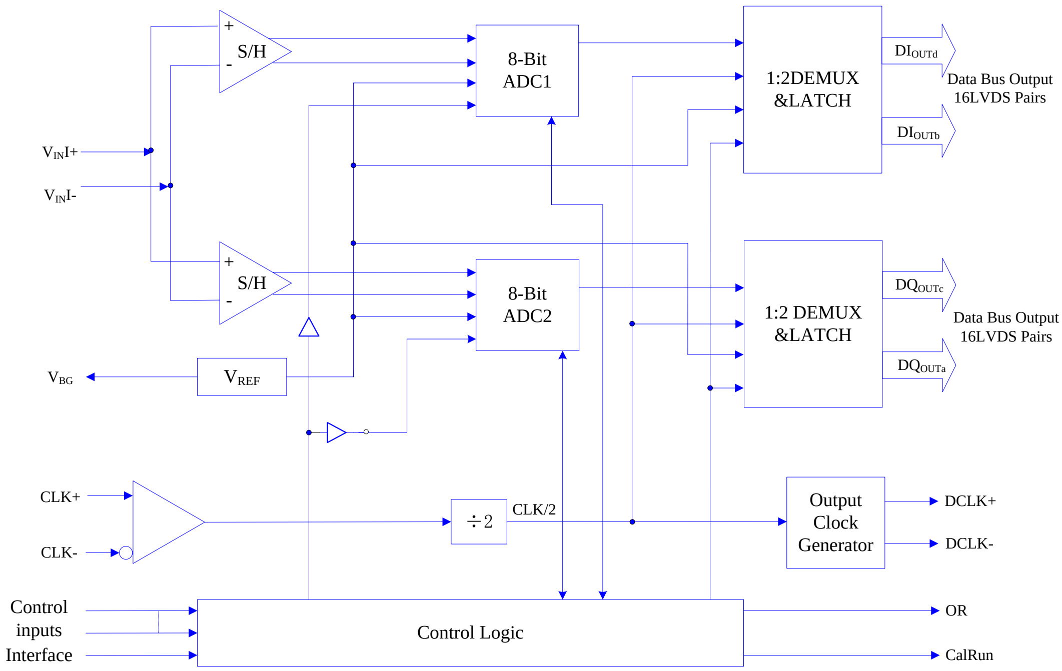


Figure 1. Block Diagram

4 Pin Description

The B083000RQC is packaged in a 128-pin ceramic quad leaded package(CQFP128). The pins description are shown in figure 2, Table1.

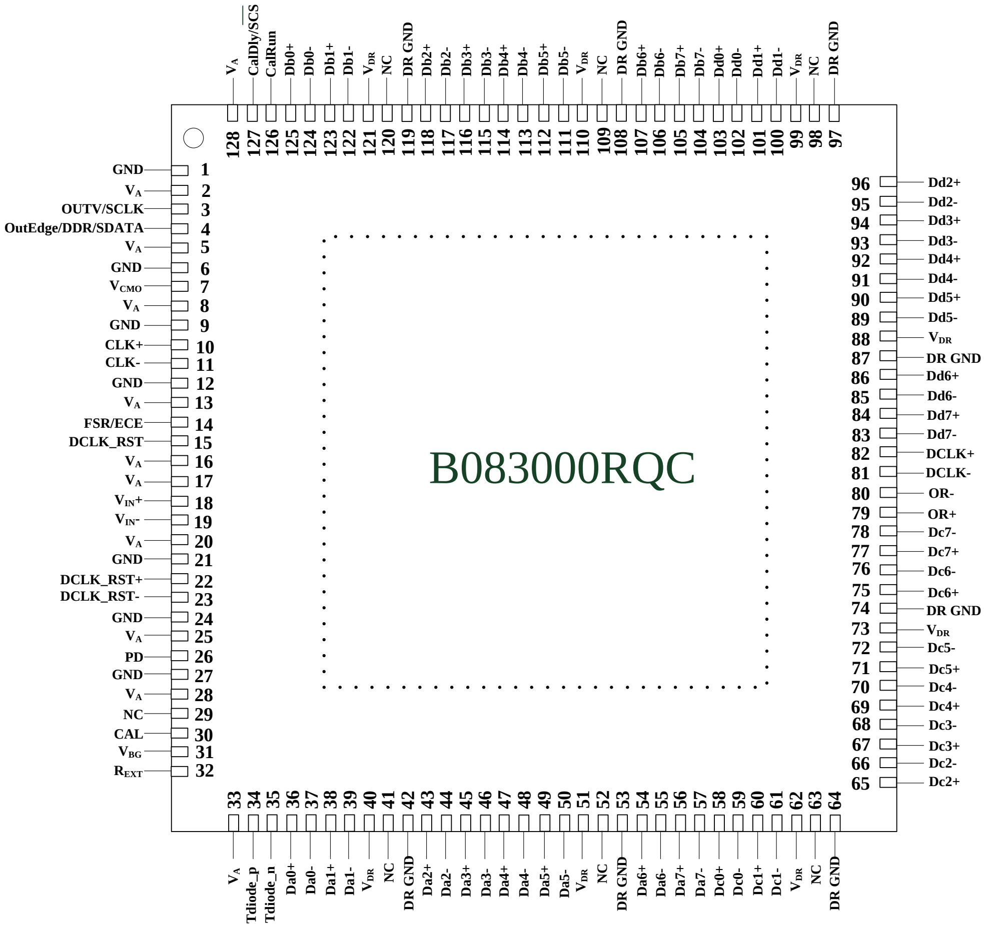


Figure2. Pin configuration

Table 1 B083000RQC Pin Description

Pin No.	Symbol	Type	Description
3	OutV/SCLK	Input(LVCMOS)	**Output Voltage Amplitude and Serial Interface Clock.** Tie this pin high for normal differential DCLK and data amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data.
4	OutEdge / DDR / SDATA	Input(LVCMOS)	**DCLK Edge Select, Double Data Rate Enable and Serial Data Input.** This input sets the output edge of DCLK+ at which the output data transitions. When this pin

Pin No.	Symbol	Type	Description
			is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. When the extended control mode is enabled, this pin functions as the SDATA input.
15	DCLK_RST	Input(LVCMOS)	**DCLK Reset** A positive pulse on this pin is used to reset and synchronize the DCLK outs of multiple converters. When bit 14 in the Configuration Register (address 1h) is set to 0b, this singleended DCLK_RST pin is selected.
26	PD	Input (LVCMOS)	**Power Down Pins.** A logic high on the PD pin puts the entire device into the Power Down Mode.
30	CAL	Input (LVCMOS)	**Calibration Cycle Initiate** A minimum 80 input clock cycles logic low followed by a minimum of 80 input clock cycles high on this pin initiates the calibration sequence.
14	FSR/ECE	Input (LVCMOS)	**Full Scale Range Select / Extended Control Enable** In non-extended control mode, a logic low on this pin sets the full-scale differential input range to 600 mV_{P-P}. A logic high on this pin sets the full-scale differential input range to 820 mV_{P-P}. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$. .
127	CalDly/$\overline{SCS}$	Input (LVCMOS)	**Calibration Delay / Serial Interface Chip Select** With a logic high or low on pin 14, this pin functions as Calibration Delay and sets the number of input clock cycles after power up before calibration begins. With pin 14 floating, this pin acts as the enable pin for the serial interface input and the CalDly value becomes "0" (short delay with no provision for a long power-up calibration delay).

Pin No.	Symbol	Type	Description
10 11	CLK+ CLK-	Input (LVDS)	**Sampling Clock Input** The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on both the rising and falling edge of CLK.
18 19	V_{IN}+ V_{IN}-	Input (Analog)	**Signal Input** The differential full-scale input range is 600mV$_{P-P}$ when the FSR pin is low, or 820mV$_{P-P}$ when the FSR pin is high. In the Extended Control Mode, FSR is determined by the Full-Scale Voltage Adjust register (address 3h, bits 15:7).
22 23	DCLK_RST+ DCLK_RST-	Input (LVDS)	**Sample Clock Reset** A positive differerntial pulse on these pins is used to reset and synchronize the DCLK outs of multiple converters. When bit 14 in the Configuration Register (address 1h) is set to 1b, these differential DCLK_RST pins are selected. See also pin 15 description.
7	V_{CMO}	Output(Analog)	**Common Mode Voltage** The voltage output at this pin is required to be the common mode input voltage at V_{IN+} and V_{IN-} when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog input. This pin is capable of sourcing or sinking 100μA and can drive a load up to 80pF.
31	V_{BG}	Output(Analog)	**Bandgap Output Voltage** Capable of 100 μA source/sink and can drive a load up to 80 pF.
126	CalRun	Output(LVCMOS)	**Calibration Running** This pin is at a logic high while a calibration is running.
32	R_{EXT}	/(Analog)	**External Bias Resistor Connection** Nominal value is 3.3k-Ohms (±0.1%) to ground.
34 35	Tdiode_P Tdiode_N	/(Analog)	**Temperature Diode** Positive (Anode) and Negative (Cathode) for die temperature measurements

Pin No.	Symbol	Type	Description
36/37 38/39 43/44 45/46 47/48 49/50 54/55 56/57 58/59 60/61 65/66 67/68 69/70 71/72 75/76 77/78	Da0+/Da0- Da1+/Da1- Da2+/Da2- Da3+/Da3- Da4+/Da4- Da5+/Da5- Da6+/Da6- Da7+/Da7- Dc0+/Dc0- Dc1+/Dc1- Dc2+/Dc2- Dc3+/Dc3- Dc4+/Dc4- Dc5+/Dc5- Dc6+/Dc6- Dc7+/Dc7-	Output(LVDS)	**A and C Data** Data Outputs from the first internal converter. The data should be extracted in the order ABCD. These outputs should always be terminated with a 100Ω differential resistor at the receiver.
84/83 86/85 90/89 92/91 94/93 96/95 101/100 103/102 105/104 107/106 112/111 114/113 116/115 118/117 123/122 125/124	Dd7+/Dd7- Dd6+/Dd6- Dd5+/Dd5- Dd4+/Dd4- Dd3+/Dd3- Dd2+/Dd2- Dd1+/Dd1- Dd0+/Dd0- Db7+/Db7- Db6+/Db6- Db5+/Db5- Db4+/Db4- Db3+/Db3- Db2+/Db2- Db1+/Db1- Db0+/Db0-	Output(LVDS)	**B and D Data** Data Outputs from the second internal converter. The data should be extracted in the order ABCD. These outputs should always be terminated with a 100Ω differential resistor at the receiver.
79 80	OR+ OR-	Output(LVDS)	**Out Of Range** A differential high at these pins indicates that the differential input is out of range (outside the range ±325 mV or ±435 mV as defined by the FSR pin). These outputs should always be terminated with a 100Ω differential resistor at the receiver.
82 81	DCLK+ DCLK-	Output(LVDS)	**Differential Clock** The Differential Clock output used to latch the output data. Delayed and non-delayed data

Pin No.	Symbol	Type	Description
			outputs are supplied synchronous to this signal. DCLK is 1/2 the sample clock rate in SDR mode and 1/4 the sample clock rate in the DDR mode. These outputs should always be terminated with a 100Ω differential resistor at the receiver. The DCLK outputs may not be active during the calibration cycle depending upon the setting of Configuration Register (address 1h), bit-14 (RTD).
2，5，8，13，16，17，20，25，28，33，128	V_A	/(Power)	**Analog power supply pins** Bypass these pins to ground.
40，51，62，73，88，99，110，121	V_{DR}	/(Power)	**Output Driver power supply pins** Bypass these pins to DR GND.
1，6，9，12，21，24，27	GND	/(Gnd)	Ground return for V_A.
42，53，64，74，87，97，108，119	DR GND	/(Gnd)	Ground return for V_{DR}.
29，41，52，63，98，109，120	NC	/	Make no connection to these pins.

5 Pin Definition（Appendix 1）

6 Function Description

The B083000RQC is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the 6.5 Section.

While it is generally poor practice to allow an active pin to float, pins 4 and 14 of the B083000RQC are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a control pin to float, connecting that pin to a potential of one half the VA supply voltage will have the same effect as allowing it to float.

6.1 Overview

The B083000RQC uses a calibrated folding and interpolating architecture that achieves 7.2 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 1.0 GSPS to 3.0 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the analog input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from the converter is below negative full scale or above positive full scale.

The B083000RQC demultiplexes the data at 1:4 and is output on all four output busses at a quarter of the ADC sampling rate. The outputs must be interleaved by the user to provide output words at the full conversion rate.

The output levels may be selected to be normal or reduced voltage. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

6.2 Transfer Characteristic

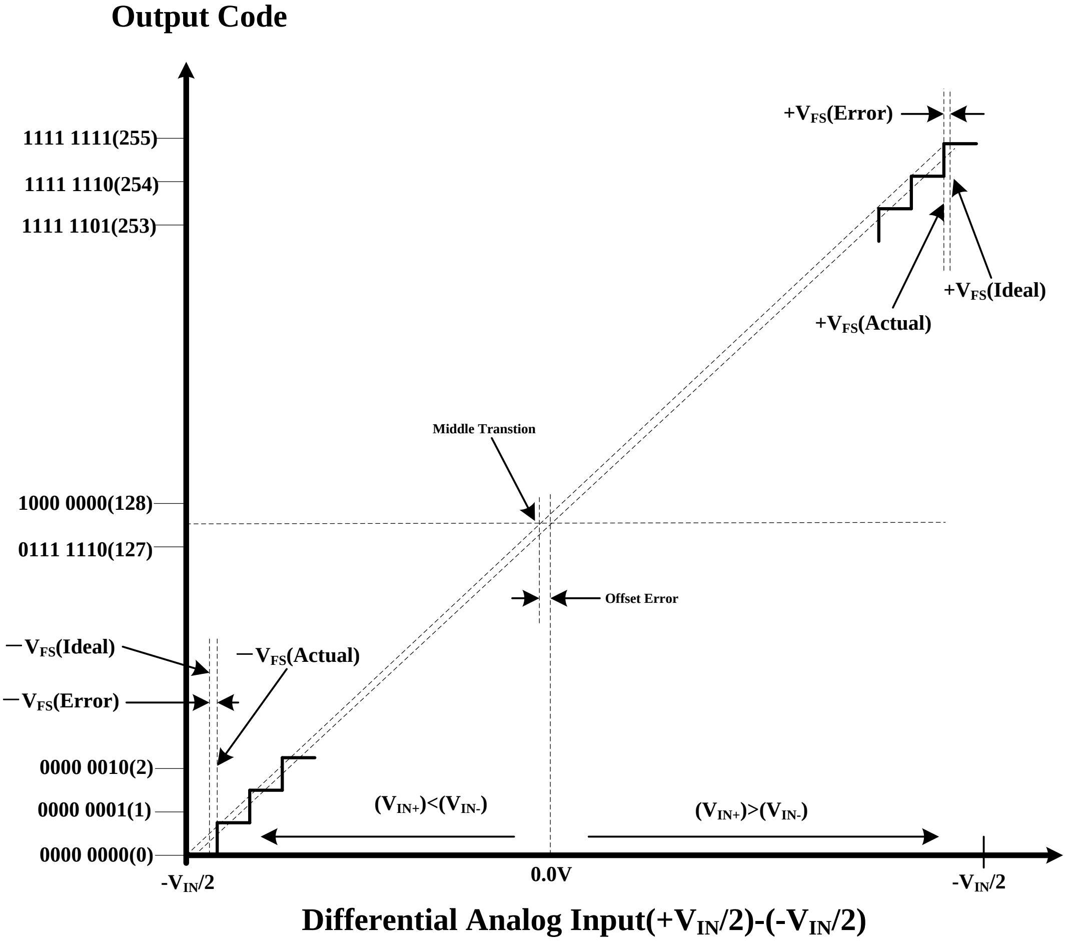


Figure3. Input / Output Transfer Characteristic

6.3 Timing Diagrams

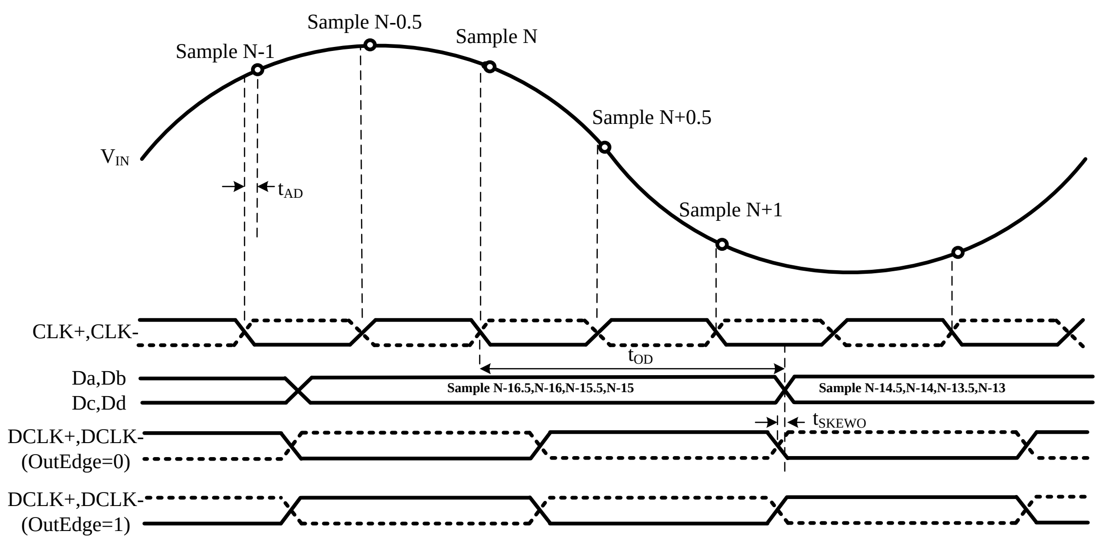


Figure4. B083000RQC Timing — SDR Clocking

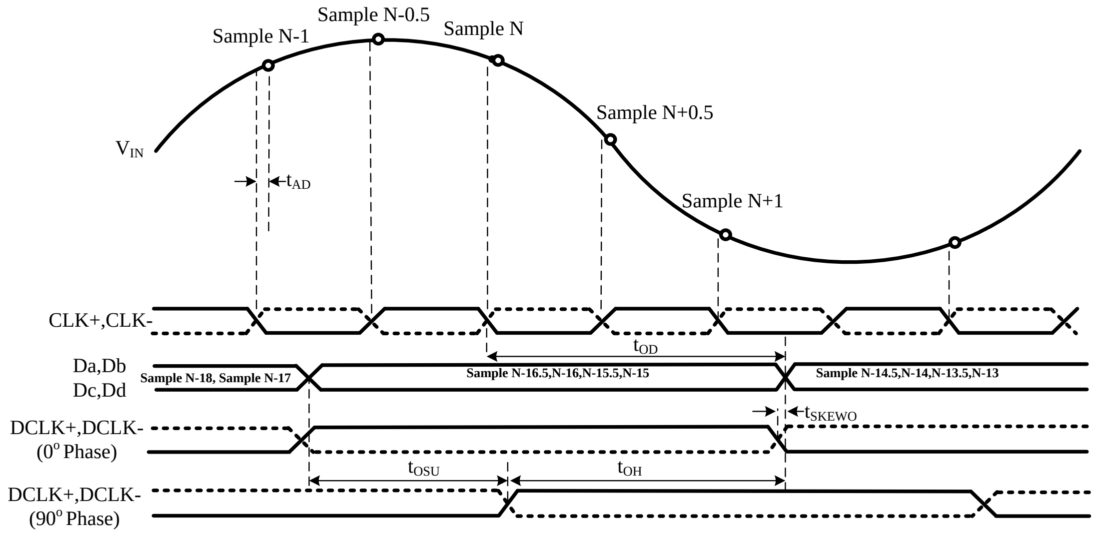


Figure5. B083000RQC Timing — DDR Clocking

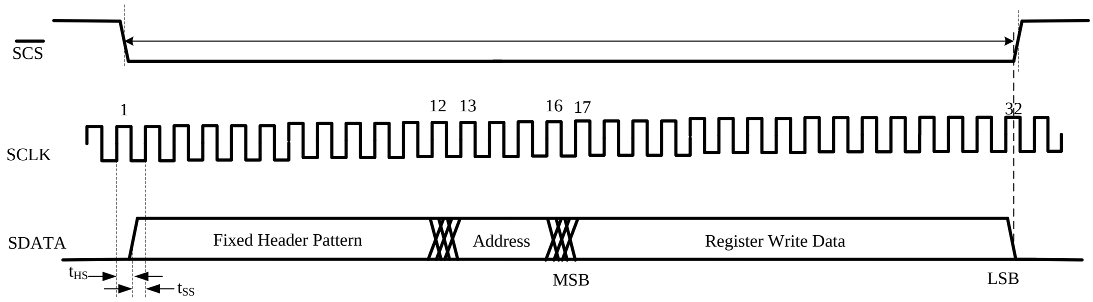


Figure6. Serial Interface Timing

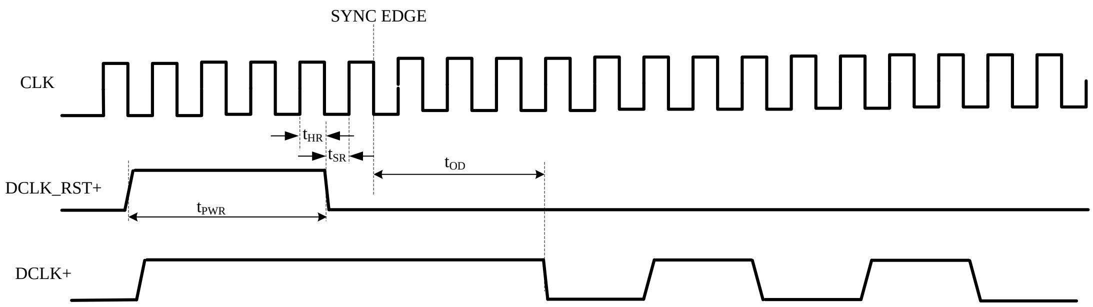


Figure7. Clock Reset Timing in DDR Mode

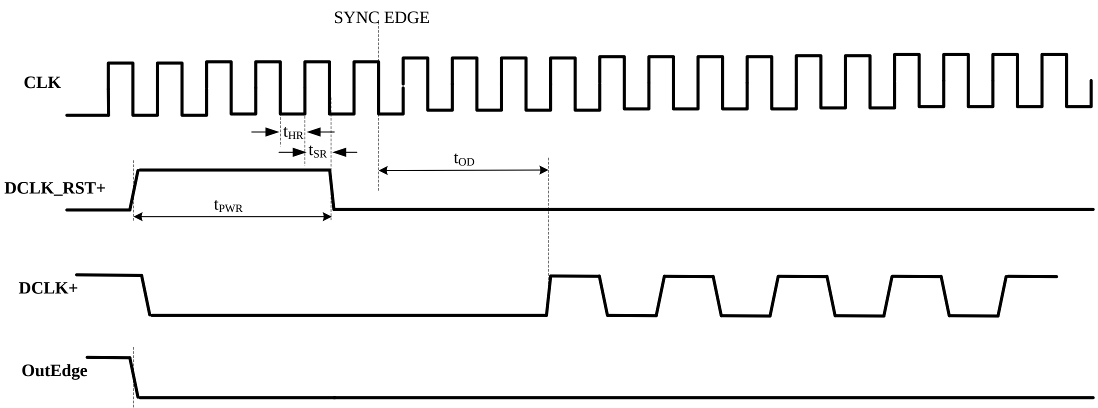


Figure8. Clock Reset Timing in SDR Mode with OUTEDGE Low

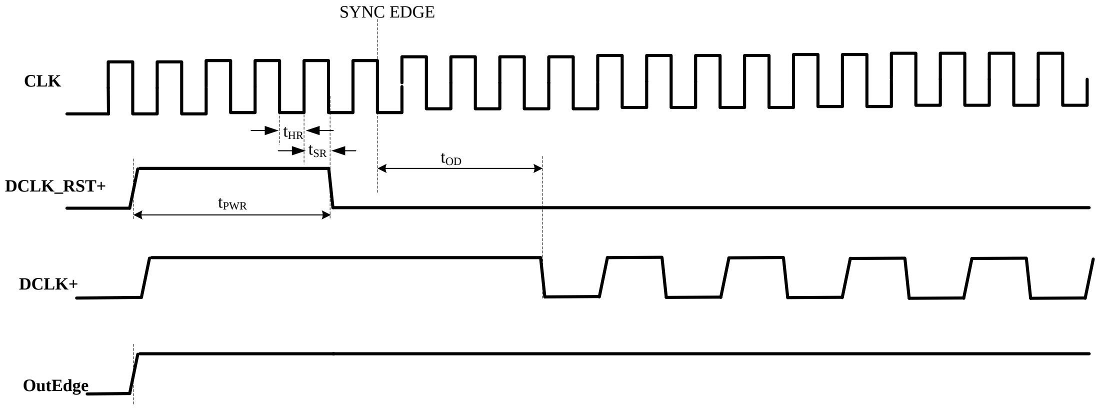


Figure9. Clock Reset Timing in SDR Mode with OUTEDGE High

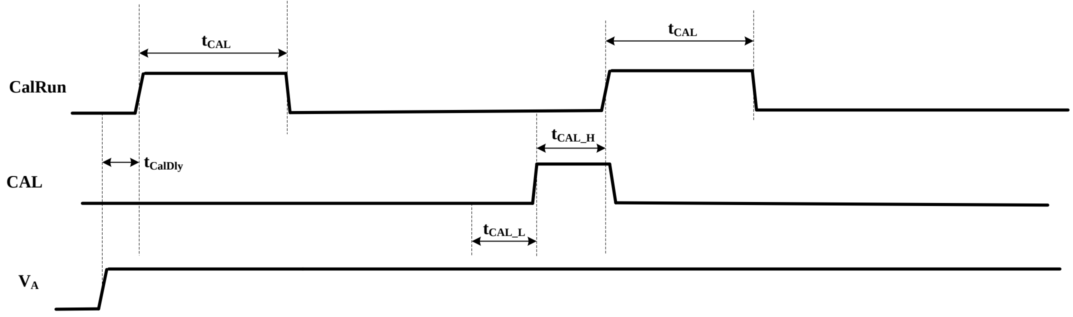


Figure10. Self Calibration and On-Command Calibration Timing

6.4 Detailed Function Description

6.4.1 Calibration

A calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, calibration must be re-run by the user whenever the state of the FSR pin is changed. For best performance, we recommend an on command calibration be run after initial power up and the device has reached a stable temperature. Also, we recommend that an on command calibration be run whenever the operating temperature changes significantly relative to the specific system performance requirements. See Section 6.5.4 for more information. Calibration can not be initiated or run while the device is in the power-down mode. See Section 6.4.7 for information on the interaction between Power Down and Calibration.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least 80 input clock cycles, then hold it high for at least another 80 input clock cycles. The time taken by the calibration procedure is specified in the A.C. Characteristics Table. Holding the CAL pin high during power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned 80 input clock cycles low followed by 80 cycles high.

CalDly (pin 127) is used to select one of two delay times after the application of power to the start of calibration. This calibration delay is 2^{25} input clock cycles (about 22 ms at 3 GSPS) with CalDly low, or 231 input clock cycles (about 1.4 seconds at 3 GSPS) with CalDly high. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the poweron settling time of the power supply.

The CAL bit does not reset itself to zero automatically, but must be manually reset before another calibration event can be initiated. If no further calibration event is desired, the CAL bit may be left high indefinitely, with no negative consequences. The RTD bit setting is critical for running a calibration event with the Clock Phase Adjust enabled. If initiating a calibration event while the Clock Phase Adjust is enabled, the RTD bit must be set to high, or no calibration will occur. If initiating a calibration event while the Clock Phase Adjust is not enabled, a normal calibration will occur, regardless of the setting of the RTD bit.

Calibration Operation Notes:

• During the calibration cycle, the OR output may be active as a result of the calibration algorithm. All data on the output pins and the OR output are invalid during the calibration cycle.

• During the power-up calibration and during the oncommand calibration when Resistor Trim Disable (address: 1h, bit 13) is not active (0b), all clocks are halted on chip, including internal clocks and DCLK, while the input termination resistor is trimmed to a value that is equal to REXT/ 33. This is to reduce noise during the input resistor calibration portion of the calibration cycle. See Section 6.5.4 for information on maintaining DCLK operation during on-command calibration. REXT is located between pin 32 and ground and must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because REXT is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of REXT should not be used.

• The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

6.4.2 Acquiring the Input

Data is acquired at both the rising and falling edges of CLK (pin 10) and the digital equivalent of that data is available at the digital outputs 13 input clock cycles later for the Dd output bus, 13.5 input clock cycles later for Dc output bus, 14 input clock cycles later for the Db output bus and 14.5 input clock cycles later for the Da output bus. See Table 2. There is an additional internal delay called t_{OD} before the data is available at the outputs. See Figure 4 and Figure 5

The B083000RQC will convert as long as the input clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with calibration, enables very good SINAD/ENOB response beyond 1.5 GHz. The B083000RQC output data signaling is LVDS and the output format is offset binary.

6.4.3 Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the B083000RQC also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with registerbased control and those pin-based controls are disabled. These pins are OutV (pin 3), OutEdge/DDR (pin 4), FSR (pin 14). See Section 6.4.8 for details on the Extended Control mode.

6.4.4 The Analog Inputs

The B083000RQC must be driven with a differential input signal. Operation with a single-ended signal is not recommended as performance will suffer. It is important that the input signals are either a.c. coupled to the inputs with the V_{CMO} pin grounded, or d.c. coupled with the V_{CMO} pin left floating or lightly loaded. An input common mode voltage equal to the V_{CMO} output must be provided when d.c. coupling is used.

Two full-scale range settings are provided with pin 14 (FSR). A high on pin 14 causes an input full-scale range setting of 820mV_{P-P}, while grounding pin 14 causes an input full-scale range setting of 600 mV_{P-P}.

In the Extended Control mode, the full-scale input range can be set to values between 560mV_{P-P} and 840 mV_{P-P} through a serial interface. See Section 6.5.2.

6.4.5 Clocking

The B083000RQC sampling clock (CLK+/CLK-) must be driven with an a.c. coupled, differential clock signal. Section 6.5..3 describes the use of the clock input pins. A differential LVDS output clock (DCLK) is available for use in latching the ADC output data into whatever device is used to receive the data.

The B083000RQC offers options for CLK+/CLK- and DCLK clocking. For DCLK, the clock edge on which output data transitions, and a choice of Single Data Rate (SDR) or Double Data Rate (DDR) outputs are available.

The sampling clock CLK has optional duty cycle correction as part of its circuit. This feature is enabled by default and provides improved ADC clocking. This circuitry allows the ADC to be clocked with a signal source having a duty cycle of 80 to 20 % (worst case).

1. **Output Demultiplexer**

The B083000RQC utilizes both the rising and falling edge of the input clock, resulting in the overall sample rate being twice the input clock frequency or 3GSPS with a 1.5 GHz input clock. The demultiplexer outputs data on each of the four output busses at 750MHz with a 1.5GHz input clock.

All data is available in parallel at the output. The four bytes of parallel data that are output with each clock is in the following sampling order, from the earliest to the latest: Da, Db, Dc, Dd. Table 2 indicates what the outputs represent for the various sampling possibilities.

The B083000RQC includes an automatic clock phase background calibration feature which automatically and continuously adjusts the phase of the ADC input clock. This feature removes the need to manually adjust the clock phase and provides optimal ENOB performance.

Table 2 Input Channel Samples Produced at Data Outputs

Data Outputs	Input/Output Relationship

Dd	ADC1 sampled with the fall of CLK, 13 cycles earlier
Db	ADC1 sampled with the fall of CLK, 14 cycles earlier
Dc	ADC2 sampled with the rise of CLK, 13.5 cycles earlier
Da	ADC2 sampled with the rise of CLK, 14.5 cycles earlier

Note: Always sourced with respect to fall of DCLK

2. OutEdge Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). This is chosen with the OutEdge input (pin 4). A high on the OutEdge input pin causes the output data to transition on the rising edge of DCLK+, while grounding this input causes the output to transition on the falling edge of DCLK+.

3. Double Data Rate

A choice of single data rate (SDR) or double data rate (DDR) output is offered. When the device is in DDR mode, address 1h, bit 8 of the Configuration Register must be set to 0b. With single data rate the output clock (DCLK) frequency is the same as the data rate of the two output buses. With double data rate the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK. DDR clocking is enabled in non-Extended Control mode by allowing pin 4 to float.

6.4.6 The LVDS Outputs

The data outputs, Out Of Range (OR) and DCLK are LVDS. Output current sources provide 3 mA of output current to a differential 100 Ohm load when the OutV input (pin 3) is high or 2.2 mA when the OutV input is low. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the B083000RQC is used is noisy, it may be necessary to tie the OutV pin high.

The LVDS data outputs have a typical common mode voltage of 800mV when the V_{BG} pin is floating. This common mode voltage can be increased to 1.150V by tying the V_{BG} pin to V_A if a higher common mode is required.

IMPORTANT NOTE: Tying the V_{BG} pin to V_A will also increase the differential LVDS output voltage (V_{OD}) by up to 40mV.

6.4.7 Power Down

The B083000RQC is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode. In this power down mode the data output pins (positive and negative) including DCLK+/- and OR +/- are put into a high impedance state and the device power consumption is reduced to a minimal level.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

6.4.8 NORMAL/EXTENDED CONTROL

The B083000RQC may be operated in one of two modes. In the Normal Mode, the user affects available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through the serial interface and a set of 6 internal registers. The two control modes are selected with pin 14 (FSR/ECE: Extended Control Enable). The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational. Table 3 shows how several of the device features are affected by the control mode chosen.

Table 3 Features and modes

Feature	Normal Control Mode	Extended Control Mode
SDR or DDR Clocking	DDR Clocking selected with pin 4 floating. SDR clocking selected when pin 4 is not floating.	Selected with nDE in the Configuration Register (1h; bit-10). When the device is in DDR mode, address 1h, bit-8 must be set to 0b.
DDR Clock Phase	Not Selectable (0 °Phase Only)	Selected with DCP bit in the Configuration Register (1h; bit-11).
SDR Data transitions with rising or falling DCLK edge	SDR Data transitions with rising edge of DCLK+ when pin 4 is high and on falling edge when low.	Selected with OE in the Configuration Register (1h; bit-8).
LVDS output level	Normal differential data and DCLK amplitude selected when pin 3 is high and reduced amplitude selected when low.	Selected with the OV in the Configuration Register (1h; bit-9).
Power-On Calibration Delay	Short delay selected when pin 127 is low and longer delay selected when high.	Short delay only.
Full-Scale Range	Selected with pin 14	Up to 512 step adjustments over a

	（600mV$_{P-P}$ or 820mV$_{P-P}$）	nominal range of 560mV to 840mV. Selected using the Input Full-Scale Adjust register (3h; bits-7 to 15).
Input Offset Adjust	Not possible	512 steps of adjustment using the Input Offset register (2h; bits-7 to 15).
Sampling Clock Phase Adjustment	The Clock Phase is adjusted automatically	The clock phase can be adjusted manually through the Fine & Coarse registers (Dh and Eh).
Test Pattern	Not Possible	A test pattern can be made present at the data outputs by selecting TPO in the Test Pattern Register (Fh; bit-11).
Resistor Trim Disable	Not Possible	The DCLK outputs will continuously be present when RTD is selected in the Configuration Register (1h; bit-13)

The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in Table 4.

Table 4. Extended Control Mode Operation (Pin 14 Floating）

Feature	**Extended Control Mode Default State**
SDR or DDR Clocking	DDR Clocking
DDR Clock Phase	Data changes with DCLK edge (0 °phase)
LVDS Output Amplitude	Normal amplitude (710 mV$_{P-P}$)
Calibration Delay	Short Delay
Full-Scale Range	700 mV nominal for both channels
Input Offset Adjust	No adjustment for either channel
Resistor Trim Disable	Trim enabled, DCLK not continuously present at output
Test Pattern	Not present at output

6.4.9 THE SERIAL INTERFACE

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$). Eight write only registers are accessible through this serial interface. Registers are write only and can not be read back.

$\overline{SCS}$：This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK：Serial data input is accepted at the rising edge of this signal. There is no minimum frequency requirement for SCLK.

SDATA：Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. SeeFigure 6.

Each Register access consists of 32 bits, as shown in Figure 6 of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. These 12 bits form the header. The next 4 bits are the address of the register thatis to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in Table 5.

Refer to the Register Description (Section 6.4.10) for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

IMPORTANT NOTE: The Serial Interface should not be accessed when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time. In the radiation condition, the serial interface is not recommended.

Table 5 Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after H0, A0 loaded last					
A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Reserved
0	0	0	1	1h	Configuration
0	0	1	0	2h	Offset

0	0	1	1	3h	Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Reserved
1	0	1	0	Ah	Reserved
1	0	1	1	Bh	Reserved
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	Extended Clock Phase adjust fine
1	1	1	0	Eh	Extended Clock Phase adjust coarse
1	1	1	1	Fh	Test Pattern

6.4.10 REGISTER DESCRIPTION

Eight write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Configuration Register

Addr：1h（0001b）　　W noly（0x92FF）

D15	D14	D13	D12	D11	D10	D9	D8
1	DRE	RTD	DCS	DCP	nDE	OV	OE

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15　Must be set to 1b

Bit 14　DRE: Differential Reset Enable. When this bit is set to 0b , it enables the single-ended DCLK_RST input. When this bit is set to 1b , it enables the differential DCLK_RST input.

POR State: 0b

Bit 13　RTD: Resistor Trim Disable. When this bit is set to 1b, the input termination resistor is not trimmed during the calibration cycle and the DCLK output remains enabled. Note that the ADC is calibrated regardless of this setting.

POR State: 0b

Bit 12 DCS: Duty Cycle Stabilizer. When this bit is set to 1b , a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled.

POR State: 1b

Bit 11 DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges ("0 °Phase"). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells ("90 ° Phase"), using the one-half speed DCLK.

POR State: 0b

Bit 10 nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Dual Data Rate) mode whereby a data word is output with each rising and falling edge of DCLK. When the device is in DDR mode, address 1h, bit-8 must be set to 0b. When this bit is set to a 1b, data bus clocking follows the SDR (single data rate) mode whereby each data word is output with either the rising or falling edge of DCLK , as determined by the OutEdge bit.

POR State: 0b

Bit 9 OV: Output Voltage. This bit determines the LVDS outputs' voltage amplitude and has the same function as the OutV pin that is used in the normal control mode. When this bit is set to 1b, the standard output amplitude of 680 mV_{P-P} is used. When this bit is set to 0b, the reduced output amplitude of 520 mV_{P-P} is used.

POR State: 1b

Bit 8 OE: Output Edge. This bit has two functions. When the device is in SDR mode, this bit selects the DCLK edge with which the data words transition and has the same effect as the OutEdge pin in the normal control mode. When this bit is set to 1b, the data outputs change with the rising edge of DCLK+. When this bit is set to 0b, the data output changes with the falling edge of DCLK+. When the device is in DDR mode, this bit must be set to 0b.

POR State: 0b

Bits 7:0 Must be set to 1b

Offset Adjust

Addr：2h（0010b） W Only（0x007F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）			Offset Value				（LSB）

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8 Offset Value. The input offset of the ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.

POR State: 0000 0000 b (no adjustment)

Bit 7 Sign bit. 0b gives positive offset, 1b gives negative offset.

POR State: 0b

Bit 6:0 Must be set to 1b

Full-Scale Voltage Adjust

Addr：3h（0011b） W Only（0x807F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）			Adjust Value				

D7	D6	D5	D4	D3	D2	D1	D0
（LSB）	1	1	1	1	1	1	1

Bit 15:7 Full Scale Voltage Adjust Value. The input fullscale voltage or gain of the ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.

0000 0000 0 560mV_{P-P}

1000 0000 0 700mV_{P-P}

Default Value

1111 1111 1 840mV_{P-P}

For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.

POR State: 1000 0000 0b

Bit 6:0 Must be set to 1b

Extended Clock Phase Adjust Fine

Addr：Dh（1101b） W Only（0x007F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）		FAM					

D7	D6	D5	D4	D3	D2	D1	D0
（LSB）	1	1	1	1	1	1	1

Bits 15:7 Fine Adjust Magnitude. With all bits set, total adjust = 110ps of non-linear clock adjust.

POR State: 000 0000 0b

Bit 6:0 Must be set to 1b

Extended Clock Phase Adjust Coarse

Addr：Eh（1110b） W Only（0x03FF）

D15	D14	D13	D12	D11	D10	D9	D8
ENA	CAM				LFS	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 Enable Clock Phase Adjust, default is 0b. RTD bit MUST also be set to ensure proper On Command Calibration with Clock Phase Adjust enabled.

Bit 14:11 Coarse Adjust Magnitude. Each LSB results in approximately 70ps of clock adjust.

POR State: 0000b

Bit 10 Low Frequency Sample clock. When this bit is set 1b, the dynamic performance of the device is improved when the sample clock is less than 900MHz.

POR State: 0b

Bit 9:0 Must be set to 1b

Test Pattern Register

Addr：Fh（1111b） W Only（0xF7FF）

D15	D14	D13	D12	D11	D10	D9	D8
1	1	1	1	TPO	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15:12 Must be set to 1b

Bit 11 TPO: Test Pattern Output enable. When this bit is set 1b, the ADC is disengaged and a test pattern generator is connected to the outputs including OR. This test pattern will work with the device in the SDR and DDR modes.

POR State: 0b

Bit 10:0 Must be set to 1b

Note Regarding Extended Mode Offset Correction

When using the Offset Adjust register, the following information should be noted.

For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure below.

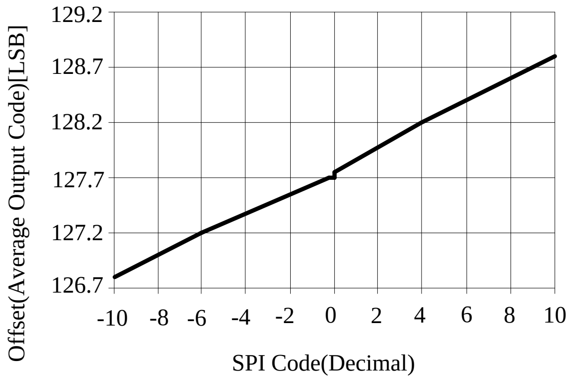


Figure 11. Extended Mode Offset Behavior

6.4.11 MULTIPLE ADC SYNCHRONIZATION

The B083000RQC has the capability to precisely reset its sampling clock (CLK) to synchronize its output clock (DCLK) and data with multiple ADCs in a system. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that they all use for sampling.

The B083000RQC has been designed to accommodate systems which require a single-ended (LVCMOS) DCLK_RST or a differential (LVDS) DCLK_RST.

Single-Ended (LVCMOS) DCLK_RST: The Power on Reset state of DCLK_RST is to have single-ended DCLK_RST activated. Bit 14, (DRE) in the Configuration Register is asserted low, 0b. When not using singled-ended DCLK_RST, the input should be grounded.

Differential (LVDS) DCLK_RST: Activated by asserting bit 14, (DRE) in the configuration register high, 1b. When the differential DCLK_RST is not activated, the inputs should be grounded. Differential DCLK_RST has an internal 100 ohm termination resistor and should not be AC coupled.

The DCLK_RST signal must observe some timing requirements that are shown in Figure 7, Figure 8 and Figure 9 of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These times are specified in the AC Electrical Characteristics Table.

The DCLK_RST signal can be asserted asynchronous to the input clock. If

DCLK_RST is asserted, the DCLK output is held in a designated state. The state in which DCLK is held during the reset period is determined by the mode of operation (SDR/DDR) and the setting of the Output Edge configuration pin or bit. (Refer to Figure 7, Figure 8 and Figure 9 for the DCLK reset state conditions). Therefore, depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted in synchronization with the CLK rising edge, the next CLK falling edge synchronizes the DCLK output with those of other B083000RQCs in the system. The DCLK output is enabled again after a constant delay (relative to the input clock frequency) which is equal to the CLK input to DCLK output delay (t_{SD}). The device always exhibits this delay characteristic in normal operation.

If the device is not programmed to allow DCLK to run continuously, DCLK will become inactive during a calibration cycle. Therefore, it is strongly recommended that DCLK only be used as a data capture clock and not as a system clock.

The DCLK_RST pin should NOT be brought high while the calibration process is running (while CalRun is high). Doing so could cause a digital glitch in the digital circuitry, resulting in corruption and invalidation of the calibration.

6.4.12 ADC TEST PATTERN

To aid in system debug, the B083000RQC has the capability of providing a test pattern at the four output ports completely independent of the input signal. The test pattern is selected by setting bit-11 (TPO) in the Test Pattern Register (address Fh). The test pattern will appear at the digital output about 10 DCLK cycles after the last write to the Test Pattern Register. The ADC is disengaged and a test pattern generator is connected to the outputs including OR. Each port is given a unique 8-bit word, alternating between 1's and 0's as described in theTable 6.

Table 6. Test Pattern by Output Port

Time	Da	Db	Dc	Dd	OR	Comments
T0	01h	02h	03h	04h	0	Pattern Sequence n
T1	FEh	FDh	FCh	FBh	1	
T2	01h	02h	03h	04h	0	
T3	FEh	FDh	FCh	FBh	1	
T4	01h	02h	03h	04h	0	
T5	FEh	FDh	FCh	FBh	1	
T6	01h	02h	03h	04h	0	

T7	FEh	FDh	FCh	FBh	1	Pattern Sequence n+1
T8	01h	02h	03h	04h	0	
T9	FEh	FDh	FCh	FBh	1	
T10	01h	02h	03h	04h	0	Pattern Sequence n+2
T11	…	…	…	…	…	

6.5 Applications Information

6.5.1 THE REFERENCE VOLTAGE

The voltage reference for the B083000RQC is derived from a 1.254V bandgap reference, a buffered version of which is made available at pin 31, V_{BG}, for user convenience. This output has an output current capability of ±100 µA. This reference voltage should be buffered if more current is required.

The internal bandgap-derived reference voltage has a nominal value of 600 mV or 820 mV, as determined by the FSR pin.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Configuration Register in the Extended Control mode.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See Section 6.5.2.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is typically 800mV when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage to a typical value of 1150mV the V_{BG} pin can be connected directly to the supply rails.

6.5.2 THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. The full-scale input range is selected with the FSR pin to be 600mV$_{P-P}$ or 820mV$_{P-P}$, or can be adjusted to values between 560mV$_{P-P}$ and 840mV$_{P-P}$ in the Extended Control mode through the Serial Interface. For best performance, it is recommended that the full-scale range be kept between 595mV$_{P-P}$ and 805mV$_{P-P}$ in the Extended Control mode because the internal DAC which sets the full-scale range is not as linear at the ends of its range.

Table 7 gives the input to output relationship with the FSR pin high when the normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in Table 7 are reduced to 75% of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

Table 7. DIFFERENTIAL INPUT TO OUTPUTRELATIONSHIP

(Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}-	Output Code
V_{CM}-205mV	V_{CM}+205mV	0000 0000
V_{CM}-102.5mV	V_{CM}+102.5mV	0100 0000
V_{CM}	V_{CM}	0111 1111/1000 0000
V_{CM}+102.5mV	V_{CM}-102.5mV	1100 0000
V_{CM}+205mV	V_{CM}-205mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

The Input impedance of V_{IN+}/V_{IN-} in the d.c. coupled mode (V_{CMO} pin not grounded) consists of a precision 100Ω resistor across the inputs and a capacitance from each of these inputsto ground. In the a.c. coupled mode, the input appears the same except there is also a resistor of 50KΩ between each analog input pin and the on-chip V_{CMO} potential. When the inputs are a.c. coupled, the V_{CMO} output must be grounded, as shown in Figure 12. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50KΩ resistors.

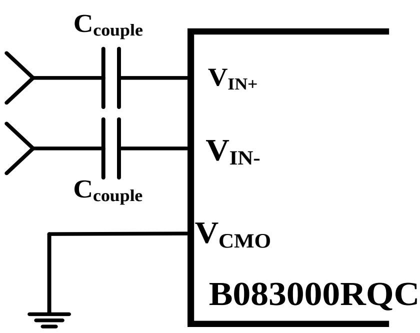


Figure12. Differential Input Drive

When the d.c. coupled mode is used, a precise common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}. Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

1. **Handling Single-Ended Input Signals**

There is no provision for the B083000RQC to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC.

2. **A.C. Coupled Input**

The easiest way to accomplish single-ended a.c. input to differential a.c. signal is with an appropriate balun, as shown in Figure 13.

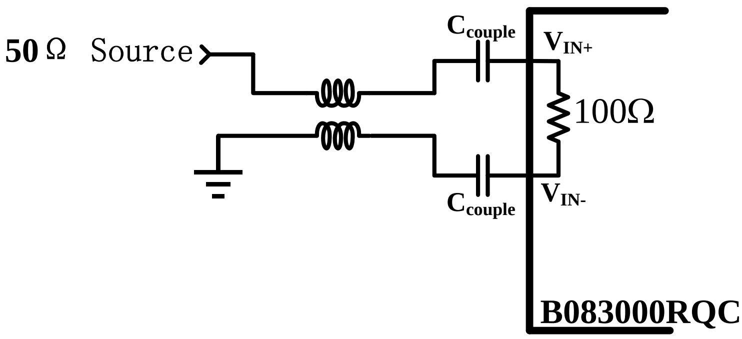


Figure13. Single-Ended to Differential Signal Conversion Using a Balun

Figure 13 is a generic depiction of a single-ended to differential signal conversion using a balun. The circuitry specific to the balun will depend on the type of balun selected and the overall board layout. It is recommended that the system designer contact the manufacturer of the balun they have selected to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, it is important to understand the input architecture of the ADC. There are specific balun parameters of which the system designer should be mindful. They should match the impedance of their analog source to the

B083000RQC's on-chip 100Ω differential input termination resistor. The range of this input termination resistor is described in the Converter Electrical Characteristics as the specification R_{IN}.

Also, as a result of the ADC architecture, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance should be no more than ±2.5° and the amplitude imbalance should be limited to less than 1dB at the desired input frequency range.

Finally, when selecting a balun, the VSWR (Voltage Standing Wave Ratio), bandwidth and insertion loss of the balun should also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss should be considered so that the signal at the balun output is within the specified input range of the ADC as described in the Converter Electrical Characteristics as the specification V_{IN}.

3. D.C. Coupled Input

When d.c. coupling to the B083000RQC analog inputs is required, single-ended to differential conversion may be easily accomplished with the LMH6555. An example of this type of circuit is shown in Figure 14. In such applications, the LMH6555 performs the task of single-ended to differential conversion while delivering low distortion and noise, as well as output balance, that supports the operation of the B083000RQC. Connecting the B083000RQC V_{CMO} pin to the V_{CM_REF} pin of the LMH6555, through an appropriate buffer, will ensure that the common mode input voltage is as needed for optimum performance of the B083000RQC. The LMV321 was chosen to buffer V_{CMO} for its low voltage operation and reasonable offset voltage.

Be sure that the current drawn from the V_{CMO} output does not exceed 100 μA.

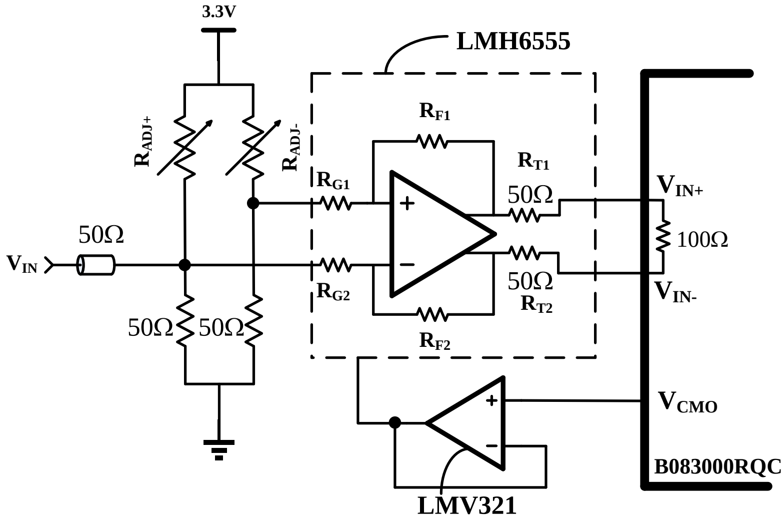


Figure14. Example of Servoing the Analog Input with V_{CMO}

In Figure 14, R_{ADJ-} and R_{ADJ+} are used to adjust the differential offset that can be measured at the ADC inputs V_{IN+}/V_{IN-}. An unadjusted positive offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ-} position. Likewise, an unadjusted negative offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ+} position. Table 8 gives suggested R_{ADJ-} and R_{ADJ+} values for various unadjusted differential offsets to bring the V_{IN+}/V_{IN-} offset back to within |15mV|.

Table 7. D.C. Coupled Offset Adjustment

Unadjusted Offset Reading	Resistor Value
0mV to 10mV	no resistor needed
11mV to 30mV	20.0kΩ
31mV to 50mV	10.0kΩ
51mV to 70mV	6.81kΩ
71mV to 90mV	4.75kΩ
91mV to 110mV	3.92kΩ

4. Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh. During a calibration cycle, the OR output is invalid.

5. Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the B083000RQC is derived from an internal band-gap reference. In the normal mode, the FSR pin controls the effective reference voltage of the B083000RQC such that the differential full-scale input range at the analog inputs is 820mV$_{P-P}$ with the FSR pin high, or is 600mV$_{P-P}$ with FSR pin low. In the Extended Control Mode, the Full Scale Range can be set anywhere from 560mV to 840mV. Best SNR is obtained with higher Full Scale Ranges, but better distortion and SFDR are obtained with lower Full Scale Ranges. The LMH6555 of Figure 14 is suitable for any Full Scale Range.

6.5.3 THE SAMPLE CLOCK INPUT

The B083000RQC has a differential LVDS clock input, CLK+/CLK-, which must be driven with an a.c. coupled, differential clock signal. Although the B083000RQC is tested and its performance is guaranteed with a differential 1.5 GHz clock, it typically will function well with input clock frequencies indicated in the Electrical Characteristics Table. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as indicated in Figure 15.

Operation up to the sample rates indicated in the Electrical Characteristics Table is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management . See Section 6.5.6.

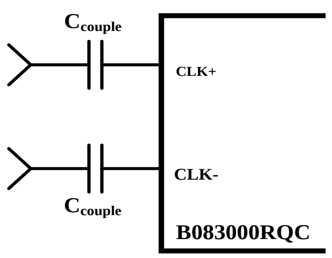


Figure15. Differential (LVDS) Input Clock Connection

The differential sample clock line pair should have a characteristic impedance of 100Ω and be terminated at the clock source in that (100Ω) characteristic impedance. The input clock line should be as short and as direct as possible. The B083000RQC clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient input clock levels will result in poor dynamic performance. Excessively high input clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the input clock level within the range specified in the Electrical Characteristics Table. The low and high times of the input clock signal can affect the performance of any A/D Converter. The B083000RQC features a duty cycle clock correction circuit which can maintain performance over temperature. The ADC will meet its performance specification if the input clock high and low times are maintained as specified in the Electrical Characteristics Table.

High speed, high performance ADCs such as the B083000RQC require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)}=(V_{INFSR}/V_{in(P-P)})\times(1/(2^{(N+1)}\times\pi\times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

Note that the maximum jitter described above is the Route Sum Square, (RSS), of the jitter from all sources, including that in the ADC input clock, that added by the system to the ADC input clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added input clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum. Input clock amplitudes above those specified in the Electrical Characteristics Table may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 128 when both input pins are at the same potential.

Manual Sample Clock Phase Adjust

The sample clock phase can be manually adjusted in the Extended Control Mode to accommodate subtle layout differences when synchronizing multiple ADCs. Register addresses Dh and Eh provide extended mode access to fine and coarse adjustments. Use of Low Frequency Sample Clock control, (register Eh; bit-10) is not supported while using manual sample clock phase adjustments.

It should be noted that by just enabling the phase adjust capability (register Eh; bit-15), degradation of dynamic performance is expected, specifically SFDR. It is intended that very small adjustments are used. Larger increases in phase adjustments will begin to affect SNR and ultimately ENOB. Therefore, the use of coarse phase adjustment should be minimized in favor of better system design.

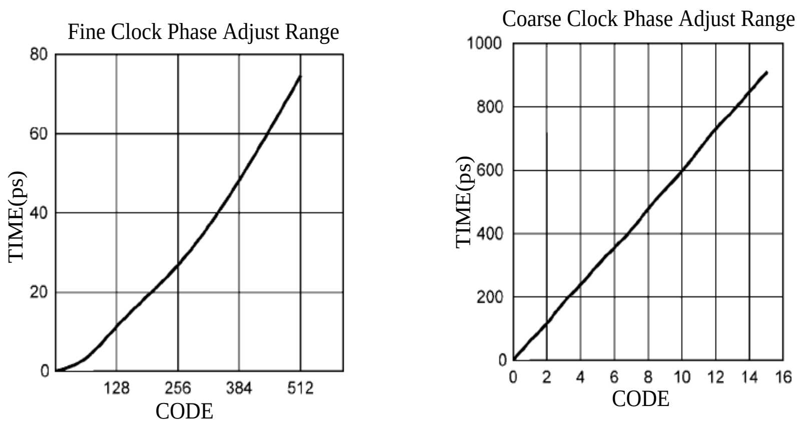


Figure16. Clock Phase Adjust

6.5.4 CONTROL PINS

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the B083000RQC and facilitate its use. These control pins provide Full-Scale Input Range setting, Calibration, Calibration Delay, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down feature.

1. **Full-Scale Input Range Setting**

The input full-scale range can be selected to be either 600mV$_{P-P}$ or 820mV$_{P-P}$, as selected with the FSR control input (pin 14) in the Normal Mode of operation. In the Extended Control Mode, the input full-scale range may be set to be anywhere from 560mV$_{P-P}$ to 840mV$_{P-P}$. See Section 6.5.2.

2. Calibration

The B083000RQC calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress. Note that the DCLK outputs are not active during a calibration cycle, therefore it is not recommended as a system clock.

3. Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, as described in the Calibration Delay Section, below.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The B083000RQC will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See On-Command Calibration Section 6.5.4.

The internal power-on calibration circuitry comes up in an unknown logic state. If the input clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 25mW. The power consumption will be normal after the clock starts.

4. On-Command Calibration

To initiate an on-command calibration, bring the CAL pin high for a minimum of 80 input clock cycles after it has been low for a minimum of 80 input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of 80 input clock cycles, then brought high for a minimum of another 80 input clock cycles. The calibration cycle will begin 80 input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum 80 input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in section 6.4.1 for best performance, a calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly relative to the specific system design performance requirements. ENOB changes slightly with increasing junction temperature and can be easily corrected by performing an on-command calibration.

5. Considerations for a continuous DCLK and proper CalRun operation：

During a Power-On calibration cycle, both the ADC and the input termination resistor are calibrated. Because dynamic performance changes slightly with junction temperature, an On-Command calibration can be executed to bring the performance of the ADC in line. By default, On-Command calibration includes calibrating the input termination resistance and the ADC. However, since the input termination resistance changes only marginally with temperature, the user has the option to disable the input termination resistor trim (address: 1h, bit: 13, set to 1b), which will guarantee that the DCLK is continuously present at the output during calibration. The Resistor Trim

Disable can be programmed in the Configuration Register (address: 1h, bit 13) when in Extended Control mode. Refer to section 6.4.10 for register programming information.

When an on-command calibration is requested while using the Aperture Adjust Circuitry through the Extended Control Mode registers, we recommend that the Resistor Trim Disable bit be set (address: 1h, bit: 13, set to 1b). This allows continuous operation of all clocks in the ADC including DCLK and proper operation of the CalRun output. The Aperture Adjust Circuitry control is resident in the Extended Control Mode registers (addresses: Dh and Eh). Refer to section 6.4.10 for register programming

Callbration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these DCLK signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that DCLK signal can be used to latch the output data into the receiving circuit.

When OutEdge (pin 4) is high, the output data is synchronized with (changes with) the rising edge of the DCLK+ (pin 82). When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the B083000RQC is capable, slight differences in the lengths of the DCLK and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK edge that best suits the application circuit and layout.

6. LVDS Output Level Control

The output level can be set to one of two levels with OutV (pin3). The strength of the output drivers is greater with OutV high. With OutV low there is less power consumption in the output drivers, but the lower output level means decreased noise immunity.

For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low. If the LVDS lines are long and/or the system in which the B083000RQC is used is noisy, it may be necessary to tie the OutV pin high.

Power Down Feature

The Power Down pin (PD) allows the B083000RQC to be entirely powered down. See Section 6.4.7 for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin for the respective channel is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

6.5.5 THE DIGITAL OUTPUTS

The B083000RQC demultiplexes the output data of each of the two ADCs on the die onto two LVDS output buses (total of four buses, two for each ADC). For each of the two converters, the results of successive conversions start on the falling edges of the CLK+ pin and are available on one of the two LVDS buses. The results of conversions that start on the rising edges of the CLK+ pin are available on the other LVDS bus. This means that the word rate at each LVDS bus is 1/2 the B083000RQC input clock rate and the two buses must be multiplexed to obtain the entire 3 GSPS conversion result.

Since the minimum recommended input clock rate for this device is 500 MHz, the sampling rate can be reduced to as low as 1 GSPS by using the results available on all four LVDS busses. The effective sampling rate can be reduced to as low as 250 MSPS by decimating the data by using one bus and a 500MHz clock.

DDR (Double Data Rate) clocking can also be used. In this mode a word of data is presented with each edge of DCLK, reducing the DCLK frequency to 1/4 the input clock frequency. When the device is in DDR mode, register address 1h, bit 8 must be set to 0b.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN+} positive with respect to V_{IN-} will produce an output code of all ones, a full-scale input level with V_{IN-} positive with respect to V_{IN+} will produce an output code of all zeros and when V_{IN+} and V_{IN-} are equal, the output code will be 128.

6.5.6 POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 μF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 μF capacitor should be placed as close as possible to each VA pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the B083000RQC should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the B083000RQC. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

1. Supply Voltage

The B083000RQC is specified to operate with a supply voltage of 1.9V±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the B083000RQC power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the B083000RQC. The circuit of Figure 17 will provide supply overshoot protection.

Many linear regulators will produce output spiking at poweron unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the B083000RQC, unless a minimum load is provided for the supply.The 100Ω resistor at the regulator output of Figure 17 provides a minimum output current during powerup to ensure there is no turn-on spiking. Whether a linear or switching regulator is used, it is advisable to provide a slow start circuit to prevent overshoot of the supply.

In the circuit of Figure 17, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended.

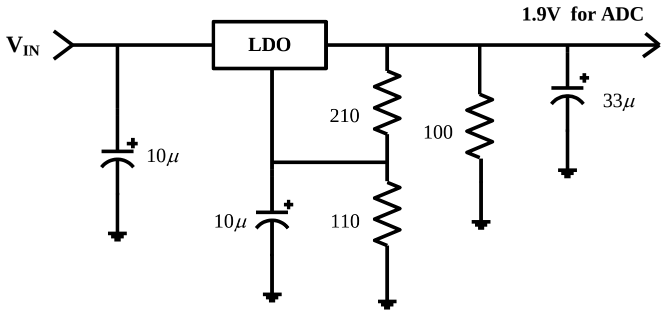


Figure 17. Non-Spliking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage and should never spike to a voltage greater than (V_A + 100mV).

If the power is applied to the device without an input clock signal present, the current drawn by the device might be below 200 mA. This is because the B083000RQC gets reset through clocked logic and its initial state is unknown. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the input clock is established.

2. Thermal Management

The B083000RQC is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 150℃. That is, TA (ambient temperature) plus ADC power consumption times θJA (junction to ambient thermal resistance) should not exceed 150℃. This is not a problem if the ambient temperature is kept to a maximum of +125℃ as specified in the Operating Ratings section and the exposed pad on the bottom of the package is thermally connected to a large enough copper area of the PC board.

Please note that the following are general recommendations for mounting exposed pad devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting. The package of the B083000RQC has an exposed pad on its back that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional CQFP, but the exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The exposed pad of the device must be soldered down to ensure adequate heat conduction out of the package. This thermal land pattern should be electrically connected to ground. A clearance of at least 0.5 mm should separate this land pattern from the mounting pads for the package pins.

6.5.7 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry. High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the B083000RQC. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

6.5.8 DYNAMIC PERFORMANCE

The B083000RQC is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in Section 6.5.3.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than offered by the package pins.

6.5.9 USING THE SERIAL INTERFACE

The B083000RQC may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. Table 8 and Table 9 describe the functions of pins 3, 4, 14 and 127 in the non-extended control mode and the extended control mode, respectively.

Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. That is, the output voltage, full-scale range and output edge selections are all controlled with pin settings. The non-extended control mode is used by setting pin 14 high or low, as opposed to letting it float. Table 8 indicates the pin functions of the B083000RQC in the nonextended control mode.

Table 8. Non-Extended Control Mode Operation(Pin 14 High or Low)

Pin	Low	High	Floating
3	$0.52V_{P-P}$ Output	$0.68V_{P-P}$ Output	n/a
4	OutEdge = Neg	OutEdge = Pos	DDR
14	$600mV_{P-P}$ Input range	$820mV_{P-P}$ Input range	Extended Control Mode
127	Caldly Low	Caldly High	Serial Interface Enable

Pin 3 can be either high or low in the non-extended control mode. Pin 14 must not be left floating to select this mode. See Section 6.4.8 for more information.

Pin 4 can be high or low or can be left floating in the nonextended control mode. In the non-extended control mode, pin 4 high or low defines the edge at which the output data transitions. See Section 6.5.4 for more information. If this pin is floating, the output clock (DCLK) is a DDR (Double Data Rate) clock (see Section 6.4.5) and the output edge synchronization is irrelevant since data is clocked out on both DCLK edges.

Pin 127, if it is high or low in the non-extended control mode, sets the calibration delay. If pin 127 is floating, the calibration delay is the same as it would be with this pin low and this pin acts as the enable pin for the serial interface input.

Table 9. Extended Control Mode Operation(Pin 14 Floating)

Pin	Function
3	SCLK（Serial Clock）
4	SDATA（Serial Data）
127	$\overline{SCS}$（Serial Interface Chip Select）

7 Absolute Maximum Ratings

Power Supply(V_A, V_{DR})..2.2 V

Supply Difference(V_A-V_{DR})..................................... 0 V~ -100 mV

Voltage on Any Input Pin(Except V_{IN+}, V_{IN-})........... -0.15 V~（V_A+0.15 V）

Voltage on V_{IN+},V_{IN-}(Maintaining Common Mode)........... -0.15 V~ 2.5 V

Ground Difference|GND-DR GND| .... 0 V~ 100 mV

Input Current at Any Pin .... ±25 mA

Package Input Current .... ±50 mA

Power Dissipation($T_A \leq 125^{\circ}C$)............................... 2.5 W

Weld Temperature(T_H, 10s)………………………………… 260 ℃

Storage Temperature (T_{stg}) ………………………………… -65 ℃ ~ +150 ℃

Junction Temperature(T_J)…………………………………… 175 ℃

8 Recommended Operating Conditions

Amblent Temperature Range ………………………… $-55\,^{\circ}C \le T_A \le +125\,^{\circ}C$

Power Supply（V_A）………………………………… +1.8V~ +2.0V

Driver Supply Power（V_{DR}）…………………………+1.8V~ V_A

Analog Input Common Mode Voltage ………………… V_{CMO} ±50mV

Voltage on V_{IN+},V_{IN-}(Maintaining Common Mode) … 200mV~ VA

Ground Difference（|GND-DR GND|）……………… 0V

CLK Pins Voltage Range ……………………………… 0V~ V_A

Differential CLK Amplitude ………………………… $0.4V_{P-P}$~$2.0V_{P-P}$

9 Radiation Hardened Performance

a) Total Ionizing Dose ≥ 100 Krad(Si);

b) SEL threshold ≥ 75 MeV cm^2/mg;

10 Package Thermal Resistance

Package	θ_{JA}	θ_{JC}（Top of Package）	θ_{J-PAD}（Thermal Pad）
128-Lead Exposed Pad CQFP	11.5 ℃/W	3.8 ℃/W	2.0 ℃/W

11 Storage Condition

The warehouse environment of B083000RQC should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of “The Space Component’s effective storage period and extended retest requirements”:

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
II	-5~30	20~75
III	-10~40	20~85

12. Electrical Characteristic

The following specifications apply after calibration for VA = VDR = $+1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential 820mVP-P, C_L = 10pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 1.5GHz at 0.5V_{P-P} with 50% duty cycle, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. Boldface limits apply for T_A = -55℃ to 125℃. All other limits T_A = 25℃, unless otherwise noted.

Table 10. Electrical Characteristic

Parameter	Symbol	Condition（Note 1,2,3）	Typ	Lim	Units (Lim)
STATIC CONVERTER CHARACTERISTICS					
Integral Non-Linearity	INL	DC Coupled, 1MHz Sine Wave Over ranged	—	**±2**	LSB(max)
Differential Non-Linearity	DNL	DC Coupled, 1MHz Sine Wave Over ranged	—	**±1**	LSB(max)
Resolution with No Missing Codes			—	**8**	Bits
Offset Error	V_{OFF}		-0.20	**±2**	LSB
Input Offset Adjustment Range	V_{OFF}-ADJ	Extended Control Mode	±45		mV
Positive Full-Scale Error	PFSE	Note 4	-1.6	**±25**	mV(max)
Negative Full-Scale Error	NFSE	Note 4	-1.0	**±25**	mV(max)
Full-Scale Adjustment Range	FS_ADJ	Extended Control Mode	±20	—	%FS
DYNAMIC CONVERTER CHARACTERISTICS					
Full Power Bandwidth	FPBW		3	—	GHz
Word Error Rate			10^{-18}	—	Errors/ Sample
Gain Flatness		0.0 to -1.0dBFS	50 to 950	—	MHz
Effective Number of Bits	ENOB	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5dB	7.2	—	Bits(min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5dB	7.0	**6.3**	Bits (min)
		f_{IN} = 1498MHz, V_{IN} = FSR − 0.5dB	6.5	—	Bits

Parameter	Symbol	Condition（Note 1,2,3）	Typ	Lim	Units (Lim)
Signal-to-Noise Plus Distortion Ratio	SINAD	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5dB	45.1	—	dB(min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5dB	43.9	**39.7**	dB(min)
		f_{IN} = 1498MHz, V_{IN} = FSR − 0.5dB	41.1	—	dB
Signal-to-Noise Ratio	SNR	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5dB	45.4	—	dB(max)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5dB	44.2	**40**	dB(max)
		f_{IN} = 1498MHz, V_{IN} = FSR − 0.5dB	41.8	—	dB
Total Harmonic Distortion	THD	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5dB	-57	—	dB(max)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5dB	-56	**-45**	dB(max)
		f_{IN} = 1498MHz, V_{IN} = FSR − 0.5dB	-49.5	—	dB
Second Harmonic Distortion	2nd Harm	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5dB	-68		dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5dB	-66	—	dB
		f_{IN} = 1498MHz, V_{IN} = FSR − 0.5dB	-56		dB
Third Harmonic Distortion	3rd Harm	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5dB	-64		dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5dB	-58	—	dB
		f_{IN} = 1498MHz, V_{IN} = FSR − 0.5dB	-52		dB

Parameter	Symbol	Condition（Note 1,2,3）	Typ	Lim	Units (Lim)
Spurious-Free dynamic Range	SFDR	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5dB	57	—	dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5dB	54.5	**45**	dB
		f_{IN} = 1498MHz, V_{IN} = FSR − 0.5dB	52.0	—	dB
Intermodulation Distortion	IMD	f_{IN} = 749.084 MHz, V_{IN} = FSR − 7dB, f_{IN} = 756.042 MHz, V_{IN} = FSR − 7dB	-52	—	dBFS
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
Full Scale Analog Differential Input Range	V_{IN}	FSR pin 14 Low	600	**550**	mVP-P (min)
				650	mVP-P (max)
		FSR pin 14 High	820	**770**	mVP-P (min)
				870	mVP-P (max)
Analog Input Common Mode Voltage	V_{CMI}		V_{CMO}	**V_{CMO}- 50**	mV(min)
				V_{CMO}+ 50	mV(max)
Analog Input Capacitance（Note 5，6）	C_{IN}	Differential	0.08		pF
		Each input pin to ground	2.2		pF
Differential Input Resistance	R_{IN}		100	**95**	Ω(min)
				105	Ω(max)
ANALOG OUTPUT CHARACTERISTICS					
Common Mode Output Voltage	V_{CMO}	I_{CMO} = ±100 μA	1.26	**0.95**	V(min)
				1.45	V(max)

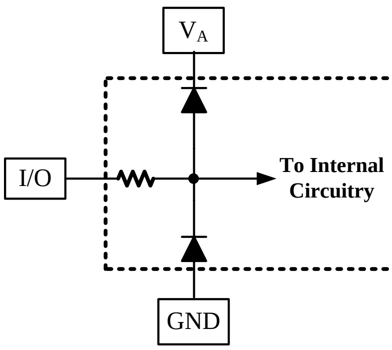
Parameter	Symbol	Condition（Note 1,2,3）	Typ	Lim	Units (Lim)
V_{CMO} input threshold to set DC Coupling mode	V_{CMO_LVL}	V_A=1.8V	0.60		V
		V_A=2.0V	0.66		V
Common Mode Output Voltage Temperature Coefficient	TC V_{CMO}	T_A = -55°C to +125°C	118		ppm/°C
Maximum V_{CMO} load Capacitance	C_{LOAD}- V_{CMO}			**80**	pF
Bandgap Reference Output Voltage	V_{BG}	I_{BG} = ±100 μA	1.26	**1.20** **1.38**	V(min) V(max)
Bandgap Reference Voltage Temperature Coefficient	TC V_{BG}	T_A = -55°C to +125°C I_{BG} = ±100 μA	28		ppm/°C
Maximum Bandgap Reference load Capacitance	C_{LOAD} V_{BG}			**80**	pF
TEMPERATURE DIODE CHARACTERISTICS					
Temperature Diode Voltage	ΔV_{BE}	192 μA vs. 12 μA, T_J=25°C	71.23		mV
		192 μA vs. 12 μA, T_J=85°C	85.54		mV
LVDS INPUT CHARACTERISTICS					
Differential Clock Input Level	V_{ID}	Sine Wave Clock	0.6	**0.4** **2.0**	V_{P-P}(min) V_{P-P}(max)
		Square Wave Clock	0.6	—	V_{P-P}(min) V_{P-P}(max)
Input Current	I_I	V_{IN}=0 or V_{IN}=V_A	±1		μA
Input Capacitance	C_{IN}	Differentia	0.02		pF
		Each input to ground	1.5		pF
LVDS OUTPUT CHARACTERISTICS					
LVDS Differential Output Voltage	V_{OD}	Measured differentially, OutV = V_A, V_{BG} = Floating (Note 7)	680	**470** **920**	mV_{P-P} (min) mV_{P-P}(max)
		Measured differentially, OutV = GND, V_{BG} = Floating (Note 7)	520	**380** **720**	mV_{P-P} (min) mV_{P-P}(max)
Change in LVDS Output Swing Between Logic Levels	$\Delta V_{O\ DIFF}$		±1		mV
Output Offset Voltage	V_{OS}	V_{BG} = Floating	800		mV

Parameter	Symbol	Condition（Note 1,2,3）	Typ	Lim	Units (Lim)
Output Offset Voltage	V_{OS}	$V_{BG}=V_A$	1150		mV
Output Offset Voltage Change Between Logic Levels	ΔV_{OS}		±1		mV
Output Short Circuit Current	I_{OS}	Output+ & Output- connected to 0.8V	±4		mA
Differential Output Impedance	Z_O		100		Ohms
LVCMOS INPUT CHARACTERISTICS					
Logic High Input Voltage	V_{IL}			**0.15× V_A**	V(max)
Logic Low Input Voltage	V_{IH}			**0.85× V_A**	V(min)
Input Capacitance	C_{IN}	Each input to ground	1.2		pF
LVCMOS OUTPUT CHARACTERISTICS					
CMOS H level output	V_{OH}	I_{OH} =-400 μA	1.65	**1.5**	V
CMOS L level output	V_{OL}	I_{OH} =400 μA	0.15	**0.3**	V
POWER SUPPLY CHARACTERISTICS					
Analog Supply Current	I_A	PD = Low	734	**840**	mA
Output Driver Supply Current	I_{DR}	PD = Low	300	**410**	mA
Power Consumption	P_D	PD = Low	1.9	**2.5**	W
		PD = High	25		mW
D.C. Power Supply Rejection Ratio	PSRR1	Change in offset with change in V_A from 1.8V to 2.0V	70		dB
A.C. Power Supply Rejection Ratio	PSRR2	248 MHz, 100mV_{P-P} riding on V_A	50		dB
AC ELECTRICAL CHARACTERISTICS - Sampling Clock					
Maximum Input Clock Frequency	f_{CLK1}	Sampling rate is 2x clock input		**1.5**	GHz（min）

Parameter	Symbol	Condition（Note 1,2,3）	Typ	Lim	Units (Lim)
Minimum Input Clock Frequency	f_{CLK2}	Sampling rate is 2x clock input	500		MHz
Input Clock Duty Cycle	t_{CYC}	500MHz ≤ Input clock frequency ≤ 1.5GHz	50	**20** **80**	%(min) %(max)
Input Clock Low Time	T_{LC}		333	**133**	ps(min)
Input Clock High Time	T_{HC}		333	**133**	ps(min)
DCLK Duty Cycle			50	**45** **55**	%(min) %(max)
Sampling (Aperture) Delay	T_{AD}		1.4		ns
Aperture Jitter	T_{AJ}		0.55		ps rms
Input Clock to Data Output Delay (in addition to Pipeline Delay)	T_{OD}	50% of Input Clock transition to 50% of Data transition	3.7		ns
Pipeline Delay		Dd Outputs		**13**	Input Clock Cycles
		Db Outputs		**14**	
		Dc Outputs		**13.5**	
		DaOutputs		**14.5**	
AC ELECTRICAL CHARACTERISTICS - Output Clock and Data					
LH Transition Time - Differential	t_{LHT}	10% to 90%	150		ps
HL Transition Time - Differential	t_{HLT}	10% to 90%	150		ps
DCLK to Data Output Skew	t_{SKEWO}	50% of DCLK transition to 50% of Data transition, SDR Mode and DDR Mode, 0 ° DCLK	±50		ps(max)
Data to DCLK Set-Up Time	t_{OSU}		570		ps
DCLK to Data Hold Time	t_{OH}		555		ps
AC ELECTRICAL CHARACTERISTICS - Serial Interface Clock					
Serial Clock Frequency	f_{SCLK}		67		MHz
Data to Serial Clock Setup Time	t_{SS}		2.5		ns(min)
Data to Serial Clock Hold Time	t_{HS}		1		ns(min)
Serial Clock Low Time				**6**	ns(min)
Serial Clock HighTime				**6**	ns(min)

Parameter	Symbol	Condition（Note 1,2,3）	Typ	Lim	Units (Lim)
AC ELECTRICAL CHARACTERISTICS – General Signals					
Setup Time DCLK_RST±	t_{SR}		90		
Hold Time DCLK_RST±	t_{HR}		30		
Pulse Width DCLK_RST±	t_{PWR}			**4**	CLK±Cyc. (min)
PD low to Rated Accuracy Conversion (Wake-Up Time)	t_{WU}		1		µs
Calibration Cycle Time	t_{CAL}		1.4×10^{5}		CLK±Cyc.
CAL Pin Low Time	t_{CAL_L}			**80**	CLK±Cyc. (min)
CAL Pin High Time	t_{CAL_H}			**80**	CLK±Cyc. (min)
Calibration delay CalDly = Low	t_{CalDly}			$\mathbf{2^{25}}$	CLK±Cyc. (min)
Calibration delay CalDly = High				$\mathbf{2^{31}}$	CLK±Cyc. (max)

Note 1: The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



Note 2: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded

Note 3: Typical figures are at TA = 25˚C, and represent most likely parametric norms.

Note 4: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error.

Note 5: The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 6: This parameter is guaranteed by design and is not tested in production.

Note 7: Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 400mv (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40mV (typical).

13 Typical Application

13.1 Typical Application（Appendix 2）

13.2 Common Application Pitfalls

Driving the inputs (analog or digital) beyond the power supply rails.

For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot. Care should be taken not to overdrive the inputs of the B083000RQC. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode.

As discussed in sections 6.4.4 and 6.5.2, the Input common mode voltage must remain within 50 mV of the V_{CMO} output , which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO} .

Using an inadequate amplifier to drive the analog input.

Use care when choosing a high frequency amplifier to drive the B083000RQC as many high speed amplifiers will have higher distortion than will the B083000RQC, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage.

As mentioned in Section 6.5.1, the reference voltage is intended to be fixed to provide one of two different full-scale values (600 mV_{P-P} and 800 mV_{P-P}). Over driving this pin will not change the full scale value, but can be used to change the LVDS common mode voltage from 0.8V to 1.15V by tying the V_{BG} pin to V_A.

Driving the clock input with an excessively high level signal.

The ADC input clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate input clock levels.

As described in Section 6.5.3, insufficient input clock levels can result in poor performance. Excessive input clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace.

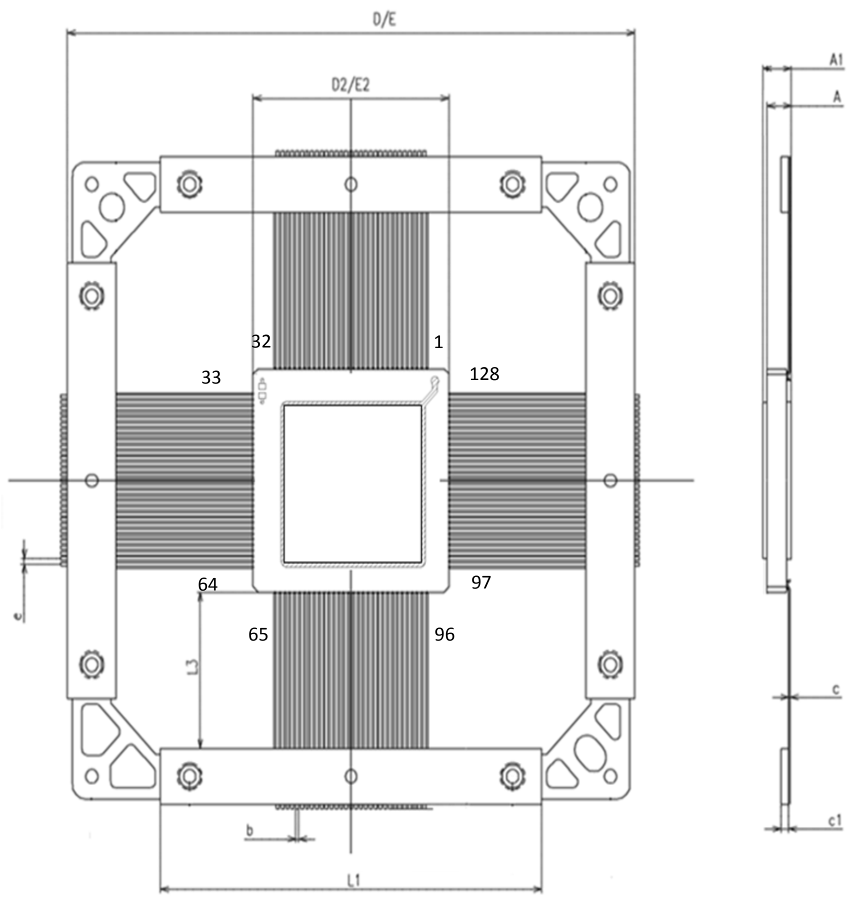
This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal.

As described in Section 6.5.6, it is important to provide adequate heat removal to ensure device reliability. This can be done either with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

14 Physical Dimensions

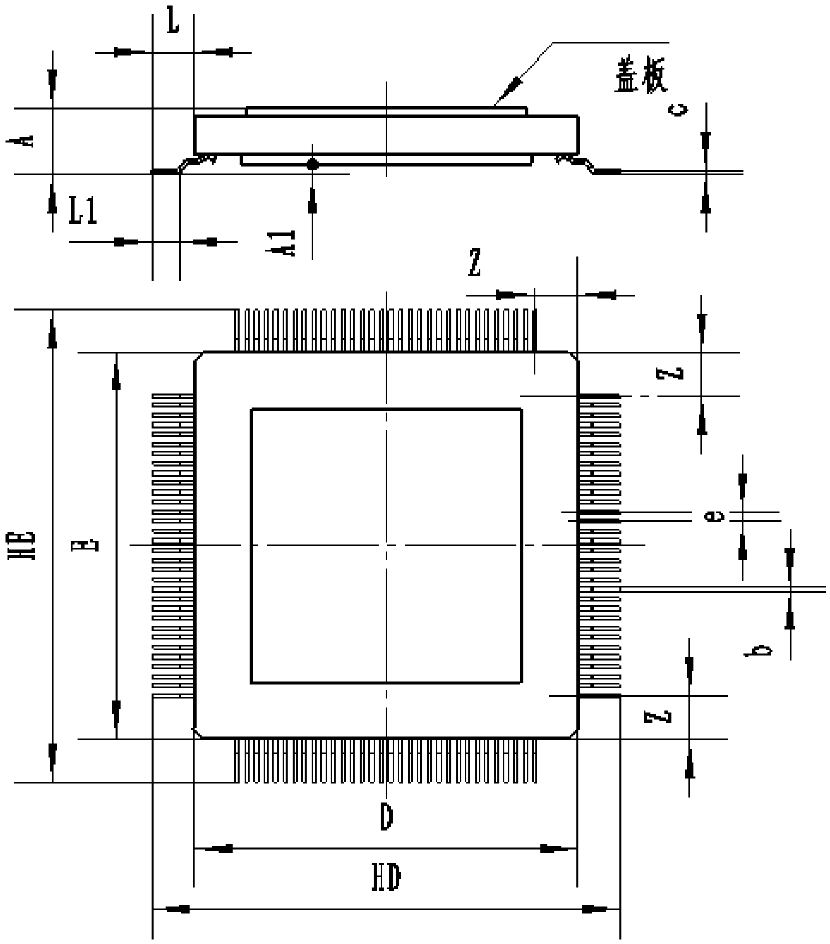
B083000RQC's package style is CQFP128, its physical size is shown in figure18.



<table>
<tr><th rowspan="2">Symbol</th><th colspan="3">Value（Units：mm）</th></tr>
<tr><th>Min</th><th>Typical</th><th>Max</th></tr>
<tr><td>A</td><td>2.25</td><td>—</td><td>2.75</td></tr>
<tr><td>A1</td><td>2.50</td><td>—</td><td>3.20</td></tr>
<tr><td>b</td><td>0.15</td><td>—</td><td>0.25</td></tr>
<tr><td>c</td><td>0.10</td><td>—</td><td>0.20</td></tr>
<tr><td>c1</td><td>—</td><td>0.80</td><td>—</td></tr>
<tr><td>D/E</td><td>57.65</td><td>—</td><td>58.35</td></tr>
<tr><td>D2/E2</td><td>19.80</td><td>—</td><td>20.20</td></tr>
<tr><td>e</td><td>—</td><td>0.50</td><td>—</td></tr>
<tr><td>L1</td><td>38.61</td><td>—</td><td>39.39</td></tr>
<tr><td>L3</td><td>13.80</td><td>—</td><td>14.20</td></tr>
</table>

Figure18. Physical size

The parameter of cut shape is met the QJ3171-2003, which is shown as follow.



Symbol	Value（Units：mm）		
	Min	Typical	Max
A	2．8	—	4．2
A1	0.5	0.75	1.0
b	—	0.2	—
c	—	0.15	—
e	—	0.5	—
Z	—	2.25	—
D/E	19.8	20	20.2
HD/HE	24.3	25.00	25.8
L1	1.25	1.5	1.75
L	2.25	2.5	2.8

Figure19. Physical size_2

Appendix 1 Pin Definition

Appendix table 1 Pin Definition

Pin NO.	Symbol	Attribute	Pin NO.	Symbol	Attribute
1	GND	Ground	**33**	V_A	Power
2	V_A	Power	**34**	Tdiode_p	Output
3	OutV/SCLK	Input	**35**	Tdiode_n	Output
4	OutEdge/DDR/SDATA	Input	**36**	Da0+	Output
5	V_A	Power	**37**	Da0-	Output
6	GND	Ground	**38**	Da1+	Output
7	V_{CMO}	Input	**39**	Da1-	Output
8	V_A	Power	**40**	V_{DR}	Power
9	GND	Ground	**41**	NC	Floating
10	CLK+	Input	**42**	DR GND	Ground
11	CLK-	Input	**43**	Da2+	Output
12	GND	Ground	**44**	Da2-	Output
13	V_A	Power	**45**	Da3+	Output

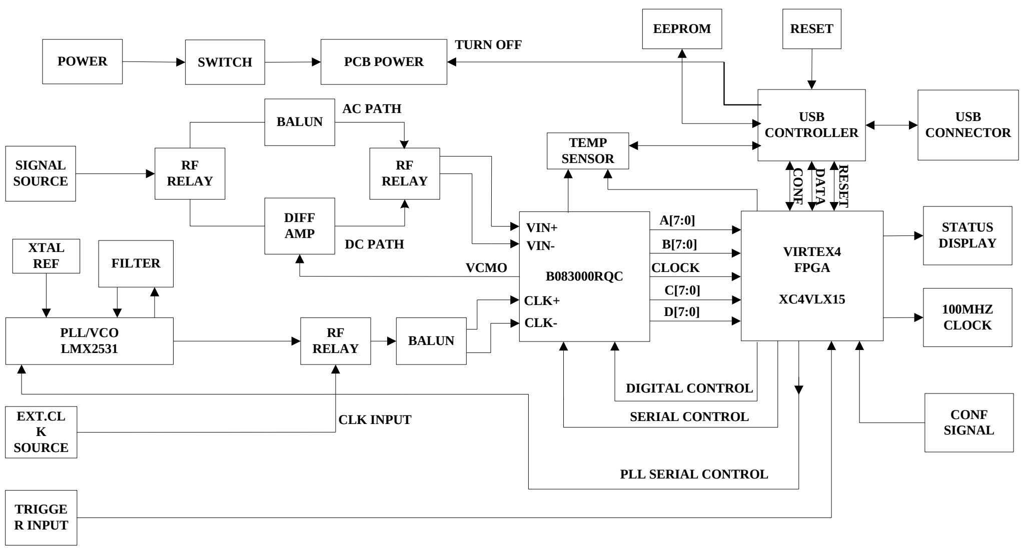
14	FSR/ECE	Input	**46**	Da3-	Output
15	DCLK_RST	Input	**47**	Da4+	Output
16	V_A	Power	**48**	Da4-	Output
17	V_A	Power	**49**	Da5+	Output
18	$V_{IN}+$	Input	**50**	Da5-	Output
19	V_{IN} -	Input	**51**	V_{DR}	Power
20	V_A	Power	**52**	NC	Floating
21	GND	Ground	**53**	DR GND	Ground
22	DCLK_RST+	Input	**54**	Da6+	Output
23	DCLK_RST-	Input	**55**	Da6-	Output
24	GND	Ground	**56**	Da7+	Output
25	V_A	Power	**57**	Da7-	Output
26	PD	Input	**58**	Dc0+	Output
27	GND	Ground	**59**	Dc0-	Output
28	V_A	Power	**60**	Dc1+	Output
29	NC	Input	**61**	Dc1-	Output
30	CAL	Input	**62**	V_{DR}	Power
31	V_{BG}	Output	**63**	NC	Floating
32	R_{EXT}	Input	**64**	DR GND	Ground

Appendix table 1(Continuous)

Pin NO.	Symbol	Attribute	Pin NO.	Symbol	Attbribute
65	Dc2+	Output	**97**	DR GND	Ground
66	Dc2-	Output	**98**	NC	Floating
67	Dc3+	Output	**99**	V_{DR}	Power
68	Dc3-	Output	**100**	Dd1-	Output
69	Dc4+	Output	**101**	Dd1+	Output
70	Dc4-	Output	**102**	Dd0-	Output
71	Dc5+	Output	**103**	Dd0+	Output
72	Dc5-	Output	**104**	Db7-	Output
73	V_{DR}	Power	**105**	Db7+	Output
74	DR GND	Ground	**106**	Db6-	Output
75	Dc6+	Output	**107**	Db6+	Output
76	Dc6-	Output	**108**	DR GND	Ground
77	Dc7+	Output	**109**	NC	Floating
78	Dc7-	Output	**110**	V_{DR}	Power

79	OR+	Output	**111**	Db5-	Output
80	OR-	Output	**112**	Db5+	Output
81	DCLK-	Output	**113**	Db4-	Output
82	DCLK+	Output	**114**	Db4+	Output
83	Dd7-	Output	**115**	Db3-	Output
84	Dd7+	Output	**116**	Db3+	Output
85	Dd6-	Output	**117**	Db2-	Output
86	Dd6+	Output	**118**	Db2+	Output
87	DR GND	Ground	**119**	DR GND	Ground
88	V_{DR}	Power	**120**	NC	Floating
89	Dd5-	Output	**121**	V_{DR}	Power
90	Dd5+	Output	**122**	Db1-	Output
91	Dd4-	Output	**123**	Db1+	Output
92	Dd4+	Output	**124**	Db0-	Output
93	Dd3-	Output	**125**	Db0+	Output
94	Dd3+	Output	**126**	CalRun	Output
95	Dd2-	Output	**127**	CalDly/$\overline{SCS}$	Input
96	Dd2+	Output	**128**	V_A	Power

Appendix 2 Typical Application



Appendix Figure 1. B083000RQC typical application circuitry

The B083000RQC'S typical application is shown in appendix figure 1. It requires only 3 connections to get started: a Power Supply, a USB Interface to a PC and an analog Signal Source. A 1.5GHz Clock generator is provided on board and the system also allows an external clock to be used if The ADC connects to a Xilinx Virtex4 FPGA which stores up to 4K of data from each channel before transferring it through the USB interface to the PC. alternative sample rates are required.

A2.1 System Description

Appendix Table 2. B083000RQC Application System Specifications

PCB Size	168mm×100mm
Power Supply	+12V，800mA
Input Clock Range	500MHz-1.5GHz
Analog Input Range(AC Couple)	30MHz-1.5GHz
Analog Input Voltage Range	600mV-820mV
Analog Input Resistance	50Ω

A2.2 Functional Description

A2.2.1 Input circuitry

The analog input signal to be digitized should be applied to the “Analog Single-Ended Input” or the “Analog Differential Input” SMA connectors. These inputs are intended to accept low-noise analog signals. To accurately evaluate the dynamic performance of this converter, the input analog signals will have to pass through a high-quality bandpass filter with at least 10-bit equivalent noise and distortion characteristics.

The single-ended input is converted to differential signals on board via a transformer connected as a balun and provides the single-ended to differential conversion for the ADC. The differential PCB traces to the ADC input pins have a characteristic differential impedance of 100 Ohms.

No scope or other test equipment should be connected anywhere in the signal path while gathering data.

The Trigger input is buffered and connected to the FPGA. The intent of this input is to allow users to expand the existing capabilities of the current system by providing an input for external triggering of a data capture. The Trigger input has no functionality in the provided FPGA firmware.

A JTAG header is available for FPGA programming and debug. The FPGA JTAG interface is also available at the Expansion Bus interface. See the Developer’s Guide for further information.

A2.2.2 ADC reference

The B083000RQC has an internal reference that can not be adjusted. However, the

Full-Scale (differential) Range may be adjusted with the Software Control Panel.

A2.2.3 ADC clock

The ADC clock is supplied on board and is fixed at 1.5GHz. An external clock signal may be applied to the ADC through the SMA Connector labeled in Appendix Figure 1 as "Clock Input". The balun-transformer (T1) converts the single ended clock source to a differential signal to drive the ADC clock pins.

Note that it is very important that the ADC clock should be as free of jitter as possible or the apparent SNR of the ADC device will be compromised.

A2.2.4 Digital Data Output

The digital output data from the ADC is connected to a Xilinx Virtex4 FPGA. Up to 4K Bytes of data per channel can be stored and then uploaded over the USB interface to the software. The FPGA logic usage is low allowing further code to be written and tested for product development.

A2.2.5 Power Requirements

The power supply requirement for the B083000RQC Evaluation Board is 12V at 800mA. Most of the regulators on board are switching regulators for increased power efficiency. The board typically draws around 500mA but it is always good practice to have extra power reserve in the power supply over the typical power requirements.

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