Ver 1.0

4000 Series FPGA

Datasheet

Part Number：B4013E

中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2018.4		Initial release	

TABLE OF CONTENTS

1. Features

- **Class level B ,certified to GJB597A and GJB548A-96**
- **Guaranteed over the full military temperature range (–55 ℃ to +125 ℃)**
- **ESD（HBM）：2KV**
- **Ceramic Packages**
- **System featured Field-Programmable Gate Arrays**
  -Select-RAMTM memory: on-chip ultra-fast RAM with
  -synchronous write option
  -dual-port RAM option
  -Fully PCI compliant (speed grades -2 and faster)
  -Abundant flip-flops -Flexible function generators -Dedicated high-speed carry logic
  -Wide edge decoders on each edge
  -Hierarchy of interconnect lines
  -Internal 3-state bus capability
  -Eight global low-skew clock or signal distribution networks
- **System Performance beyond 80 MHz**
- **Flexible Array Architecture**
- **Low Power Segmented Routing Architecture**
- **Systems-Oriented Features**
  -IEEE 1149.1-compatible boundary scan logic support
  -Individually programmable output slew rate
  -Programmable input pull-up or pull-down resistors
  -12 mA sink current per B4013EE output
- **Configured by Loading Binary File**
  -Unlimited re-programmability
- **Read Back Capability**
  -Program verification
  -Internal node observability
- **Backward Compatible with B4013E Devices**
- **Development System runs on most common computer platforms**
  -Interfaces to popular design environments
  -Fully automatic mapping, placement and routing
  -Interactive design editor for design optimization
- **0.5 um 3-layer metal process**
- **100% factory tested**
- **Compatibility of XQ4013E FPGA**
  -Be compatible with XQ4013E FPGA of Xilinx

2. General Description

B4013E FPGA high-performance, high-capacity Field Pro-grammable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs com-bine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

The B4013E is shown as Table 1.

Table 1: B4013E Field Programmable Gate Array

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
B4013E	1368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	CLCC132 CPGA223

3. Block Diagram

Description

Figure 1 shows B4013E device's diagram.The device is implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

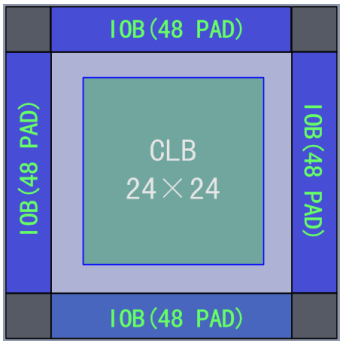


Figure 1 B4013E device's diagram

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave and peripheral modes).

B4013E FPGAs are supported by powerful and sophisticated software, covering every aspect of design from schematic or behavioral entry, floor planning, simula-tion, automatic block placement and routing of intercon-nects, to the creation, downloading, and readback of the configuration bit stream.

Because BMTI FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hard-ware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a

cost-effective solution for produc-tion rates well beyond 5,000 systems per month. For lowest high-volume unit cost, a design can first be implemented in the B4013EE or B4013EX, then migrated to one of BMTI's compatible HardWire mask-programmed devices.

Taking Advantage of Re-configuration

FPGA devices can be re-configured to change logic func-tion while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be re-con-figured dynamically to perform different functions at differ-ent times.

Re-configurable logic can be used to implement system self-diagnostics, create systems capable of being re-con-figured for different environments or operations, or imple-ment multi-purpose hardware for a given application. As an added benefit, using re-configurable FPGA devices simpli-fies hardware design and debugging and shortens product time-to-market.

4. Pin Description

There are three types of pins in the B4013E Device:

- Permanently dedicated pins

- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 kΩ -100 kΩ pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 kΩ - 100 kΩ pull-up resistor.

B4013E device have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR.

B4013E device have no Powerdown control input. For B4013E device, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode.

Device pins for B4013E device are described in Table 1. Pin functions during configuration for each of the seven configuration modes are summarized in Table 2, in the "Configuration Timing" section.

Table2: Special Purpose Pins

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
VCC	I	I	Eight or more (depending on package type) connections to the nominal +5 V supply voltage. Must be decoupled with a 0.01 - 0.1 µF capacitor to Ground.
GND	I	I	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master modes or Asyn-chronous Peripheral mode, but is an input in Slave mode and Synchronous Peripheral mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on B4013E device, except during Readback.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the XACTstep program that creates the configuration bitstream. The resistor is included by default.

PROGRAM	I	I	PROGRAM is an active Low input that forces the FPGA to clear its configuration mem-ory. It is used to initiate a configuration cycle. When PROGRAM goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases INIT. The PROGRAM pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
User I/O Pins That Can Have Special Functions			
RDY/BUSY	O	I/O	During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asyn-chronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/BUSY is a user-programmable I/O pin. RDY/BUSY is pulled High with a high-impedance pull-up prior to INIT going High.
M0, M1, M2	I	I (M0), O (M1), I (M2)	As Mode inputs, these pins are sampled after INIT goes High to determine the configu-ration mode to be used. After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers. During configuration, these pins have weak pull-up resistors. For the most popular con-figuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down re-sistors. A pull-down resistor value of 4.7 kΩ is recommended. These pins can only be used as inputs or outputs when called out by special schematic definitions. To use these pins, place the library components MD0, MD1, and MD2 in-stead of the usual pad symbols. Input or output buffers must still be used.
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhib-ited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. In-put or output buffers must still be used.

HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
LDC	O	I/O	Low During Configuration (LDC) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, LDC is a user-programmable I/O pin.
INIT	I/O	I/O	Before and during configuration, INIT is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, INIT is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after INIT has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, INIT is a user-programmable I/O pin.
CS0, CS1, WS, RS	I	I/O	These four inputs are used in Asynchronous Peripheral mode. The chip is selected when CS0 is Low and CS1 is High. While the chip is selected, a Low on Write Strobe (WS) loads the data present on the D0 - D7 inputs into the internal data buffer. A Low on Read Strobe (RS) changes D7 into a status output — High if Ready, Low if Busy — and drives D0 - D6 High. In Express mode, CS1 is used as a serial-enable signal for daisy-chaining. WS and RS should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.
D0 - D7	I	I/O	During Master Parallel and Peripheral configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. During Parallel configuration, DIN is the D0 input. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During configuration in any mode but Express mode, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Express modefor B4013EE and B4013EX only, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.

Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resis-tor (25 kΩ - 100 kΩ) that defines the logic level as High.

5. Pin Configurations

See Appendix 1.

Table 3 :B4013E Package Combinations and Maximum I/O

Device	Package	Maximum I/O	Pin configuration
B4013E	CLCC132	102	Appendix 1
	CPGA223	192	Appendix 1

6. Product Description

XC4000 Series devices achieve high speed through advanced semiconductor technology and improved architecture.The XC4000E and XC4000X support system clock rates of up to 80 MHz and internal performance in excess of 150 MHz. Compared to older Xilinx FPGA families, XC4000 Series devices are more powerful. They offer on-chip edge-triggered and dual-port RAM, clock enables on I/O flip-flops, and wide-input decoders. They are more versatile in many applications, especially those involving RAM. Design cycles are faster due to a combination of increased routing resources and more sophisticated software.

Basic Building Blocks

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing the user’s logic.
- IOBs provide the interface between the package pins and internal signal lines.Three other types of circuits are also available:
- 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
- Wide edge decoders are available around the periphery of each device.

- An on-chip oscillator is provided.

Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks.The functionality of each circuit block is customized during configuration by programming internal static memory cells.The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. Each of these available circuits is described in this section.

Refer to the "XC4000E and XC4000X Series Field Programmable Gate Arrays" commercial data sheet for more information on device architecture and timing specifications.

7. Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. B4013E device use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACTstep development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary connections. M2 and M0 can be used as inputs, and M1 can be used as an output. The XACTstep development sys-tem does not use these resources unless they are explicitly specified in the design entry. This is done by placing a spe-cial pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In B4013E Device, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most com-mon configuration mode, the mode pins can be left uncon-nected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can

individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets.

Configuration Modes

B4013E device have six configuration modes. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The coding for mode selection is shown in Table 4

Table 4: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide

Master Modes

The three Master modes use an internal oscillator to gener-ate a Configuration Clock (CCLK) for driving potential slave devices.They also generate address and timing for exter-nal PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF (3FFFFF when 22 address lines are used), for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a BMTI serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow fre-quency, then can switch to the higher frequency

during the first frame. Frequency tolerance is -50% to +25%.

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configura-tion data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be con-nected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configura-tion bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained con-figuration.

8. Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin.

There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the sub-sequent rising CCLK edge.

Figure 2 shows a full master/slave system. An B4013E Series device in Slave Serial mode should be connected as shown in the third device from the left. Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resis-tors during configuration.

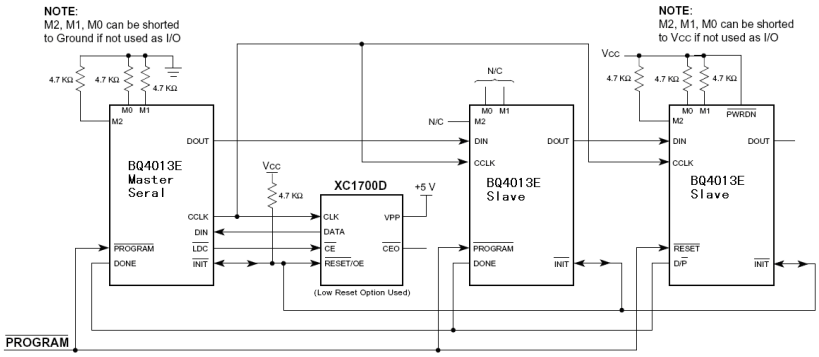
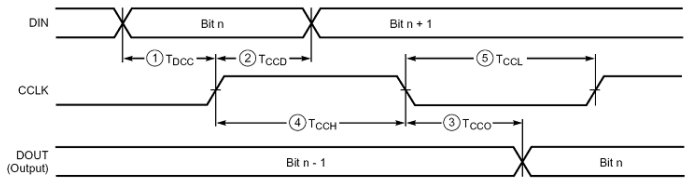


Figure 2: Master/Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 3: Slave Serial Mode Programming Switching Characteristics

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a BMTI Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the

SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

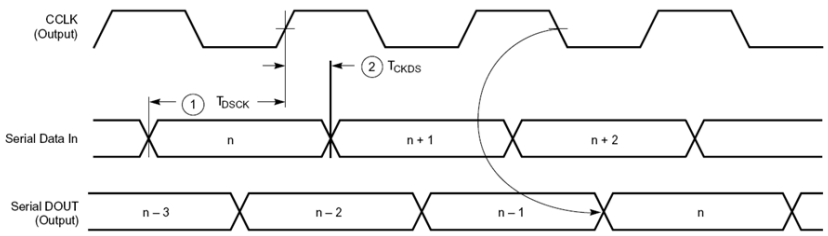
The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In the bitstream generation software, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight.

For actual timing values please refer to “Configuration Switching Characteristics” on page 68. Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either LDC or DONE. Using LDC avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but LDC is then restricted to be a permanently High user output after con-figuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Figure 2 shows a full master/slave system. The leftmost device is in Master Serial mode. Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DSCK}	20		ns
	DIN hold	2	T_{CKDS}	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 4: Master Serial Mode Programming Switching Characteristics

Master Parallel Modes

In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decre-menting the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that over-flows the lead device—on its DOUT pin. There is

an inter-nal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

The PROM address pins can be incremented or decre-mented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of

microprocessors and micro controllers. Some processors must boot from the bottom of memory (all zeros) while oth-ers must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the mem-ory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at 3FFFF and decrement.

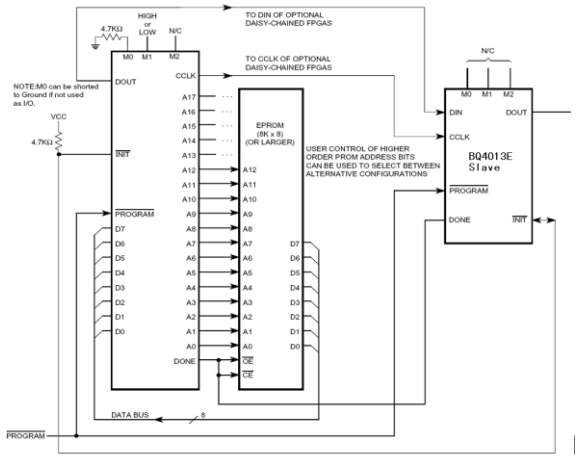
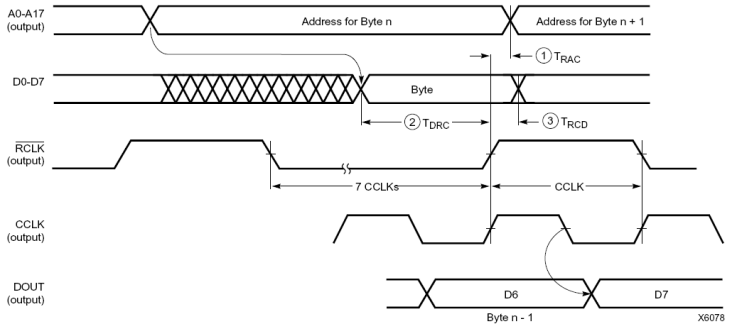


Figure 5: Master Parallel Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
RCLK	Delay to Address valid	1	T_{RAC}	0	200	ns
	Data setup time	2	T_{DRC}	60		ns
	Data hold time	3	T_{RCD}	0		ns

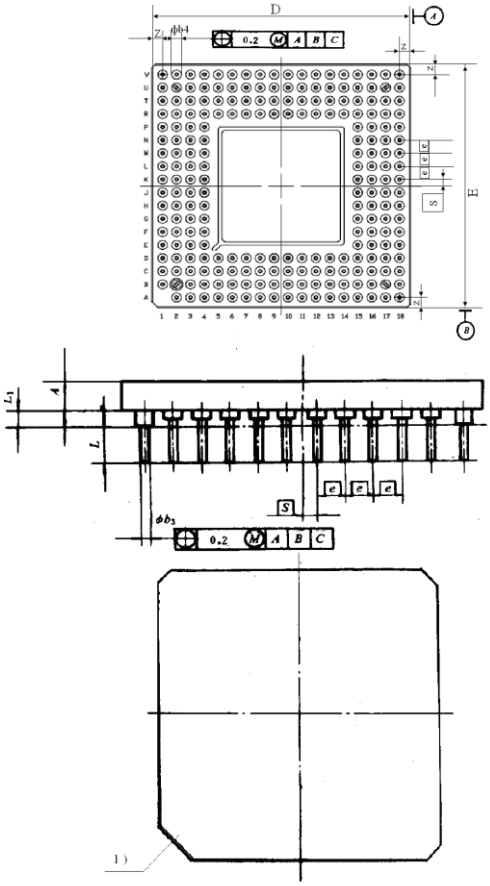
Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until Vcc is valid.
2. The first Data byte is loaded and CCLK starts at the end of the first RCLK active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Figure 6: Master Parallel Mode Programming Switching Characteristics

9. Package

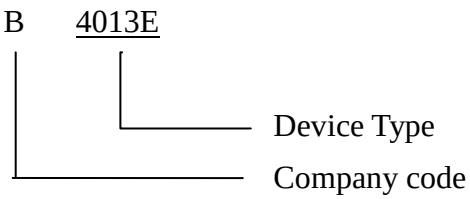
B4013E Pin Function Diagram



B4013E CPGA223 Package view

SIGN	MIN（mm）	MON（mm）	MAX（mm）
A	——	——	3.30
ϕb3	0.41	——	0.50
ϕb4	1.65	——	1.91
e	——	2.54	——
L	2.54	——	5.08
L_1	1.02	——	1.52
Z	——	——	2.29
D	46.74	——	47.74
E	46.74	——	47.74

Naming Rule



Replaced Product

Device Type	Substituted Device Type
B4013E	Xilinx　XQ4013E-4PG223M

Appendix 1

Table 1　B4013E Pinout Tables (CPGA223)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A2	I/O（TDI）	D1	I/O	J4	Vcc	R9	GND
A3	I/O	D2	I/O（A13）	J15	Vcc	R10	Vcc
A4	I/O	D3	Vcc	J16	I/O（INIT）	R11	I/O
A5	I/O	D4	GND	J17	I/O	R12	I/O
A6	I/O	D5	I/O	J18	I/O	R13	I/O
A7	I/O	D6	I/O	K1	I/O	R14	I/O
A8	I/O	D7	I/O	K2	I/O（A6）	R15	Vcc
A9	I/O	D8	I/O	K3	I/O（A7）	R16	GND
A10	I/O	D9	GND	K4	GND	R17	I/O
A11	I/O	D10	Vcc	K15	GND	R18	I/O
A12	I/O	D11	I/O	K16	I/O	T1	I/O
A13	I/O	D12	I/O	K17	I/O	T2	I/O（CS1，A2）
A14	I/O	D13	I/O	K18	I/O	T3	I/O（A0，WS）
A15	I/O	D14	I/O	L1	I/O	T4	SGCK4（DOUT，I/O）
A16	I/O	D15	GND	L2	I/O	T5	I/O
A17	I/O	D16	Vcc	L3	I/O	T6	I/O
A18	M0	D17	I/O	L4	I/O	T7	GND
B1	I/O	D18	I/O	L15	I/O	T8	I/O
B2	SGCK1（A15，I/O）	E1	I/O	L16	I/O	T9	I/O（D3）
B3	I/O	E2	I/O	L17	I/O	T10	I/O
B4	I/O（TCK）	E3	I/O	L18	I/O	T11	I/O
B5	I/O	E4	I/O	M1	I/O（A5）	T12	GND
B6	I/O	E15	I/O	M2	I/O（A4）	T13	I/O
B7	I/O（TMS）	E16	I/O（HDC）	M3	GND	T14	I/O
B8	I/O	E17	I/O（LDC）	M4	I/O	T15	I/O（D7）
B9	I/O	E18	I/O	M15	I/O	T16	SGCK3（I/O）
B10	I/O	F1	I/O	M16	GND	T17	I/O
B11	I/O	F2	I/O	M17	I/O	T18	I/O
B12	I/O	F3	I/O（A12）	M18	I/O	U1	PGCK4（I/O，A1）
B13	I/O	F4	I/O	N1	I/O	U2	TD0
B14	I/O	F15	I/O	N2	I/O	U3	I/O（D0，DIN）
B15	I/O	F16	I/O	N3	I/O（A3）	U4	I/O
B16	SGCK2（I/O）	F17	I/O	N4	I/O	U5	I/O
B17	PGCK2（I/O）	F18	I/O	N15	I/O	U6	I/O
B18	I/O	G1	I/O（A10）	N16	I/O	U7	I/O
C1	I/O	G2	I/O（A11）	N17	I/O	U8	I/O
C2	I/O（A14）	G3	GND	N18	I/O	U9	I/O（RS）
C3	PGCK1（A16，I/O）	G4	I/O	P1	I/O	U10	I/O（D4）
C4	I/O（A17）	G15	I/O	P2	I/O	U11	I/O
C5	I/O	G16	GND	P3	I/O	U12	I/O（D5）
C6	I/O	G17	I/O	P4	I/O	U13	I/O
C7	GND	G18	I/O	P15	I/O	V8	I/O
C8	I/O	H1	I/O	P16	I/O	V9	I/O
C9	I/O	H2	I/O	P17	I/O	V10	I/O
C10	I/O	H3	I/O	P18	I/O	V11	I/O
C11	I/O	H4	I/O	R1	I/O	V12	I/O（CS0）
C12	GND	H15	I/O	R2	I/O	V13	I/O
C13	I/O	H16	I/O	R3	GND	V14	I/O

C14	I/O	H17	I/O	R4	Vcc	V15	I/O
C15	M1	H18	I/O	R5	I/O	V16	I/O
C16	M2	J1	I/O	R6	I/O	V17	I/O（D6）
C17	I/O	J2	I/O（A9）	R7	I/O	V18	PROGRAM
C18	I/O	J3	I/O（A8）	R8	I/O		

Service and Support：

Address:No.2 Siyingmen N. Road. Donggaodi. Fengtai District.Beijing.China.

Department:Department of international cooperation

Telephone:+86(0)10-67968115-7178

Email:gjhz@mxtronics.com

Fax:+86(0)10-68757706

Zip code:100076