Ver 1.1

Radiation-Hardened QUAD DRIVER

Datasheet

Part Number：B54LVDSC031RH

中国航天 北京微电子技术研究所

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	20110320	——	——	
1.1	20180313	——	change version	

TABLE OF CONTENTS

1. Features

- >155.5 Mbps (77.7 MHz) switching rates
- +350mV nominal differential signaling
- 5 V power supply
- Cold Spare LVDS outputs
- TTL compatible inputs
- Ultra low power CMOS technology
- 5.0ns maximum, propagation delay
- 3.0ns maximum, differential skew
- Radiation-hardened design：
  - Total-dose: 300 krad(Si)
  - Latchup (LET >75MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack
- Compatible with IEEE 1596.3SCI LVDS

  Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard

2. General Description

The B54LVDSC031RH Quad Driver is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps(77.7 MHz) utilizing Low Voltage Differential Signaling(LVDS) technology. The B54LVDSC031RH accepts TTL input levels and translates them to low voltage (340mV) differential output signals. In addition, the driver supports a three-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device toan ultra low idle power state. The B54LVDSC031RH and companion quad line receiver B54LVDS032RH provide new alternatives to high

power pseudo-ECL devices for high speed point-to-point interface applications. Quad Driver is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps(77.7 MHz) utilizing Low Voltage Differential Signaling(LVDS) technology. The B54LVDSC031RH accepts TTL input levels and translates them to low voltage (340mV) differential output signals. In addition, the driver supports a three-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device toan ultra low idle power state. The B54LVDSC031RH and companion quad line receiver B54LVDS032RH provide new alternatives to high power pseudo-ECL devices for high speed point-to-point interface applications.

All LVDS pins have Cold Spare buffers. These buffers willbe high impedance when VDD is tied to VSS.

3. Function Block Diagram

B54LVDSC031RH function block diagram is shown in figure 3-1.

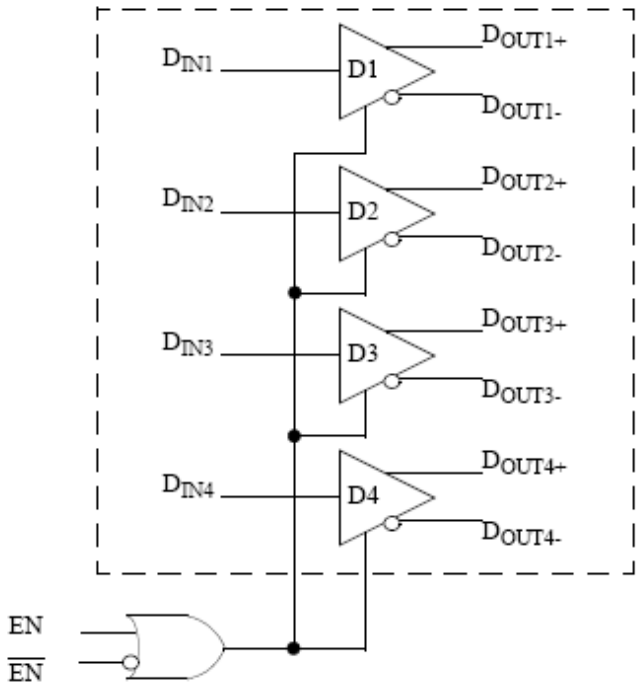


Figure 3-1 B54LVDSC031RH function block digram

4. Packages and Pin Function Descriptions

The provided package is: FP16 and DIP16

B54LVDSC031RH - pin configuration is shown in 4-1.

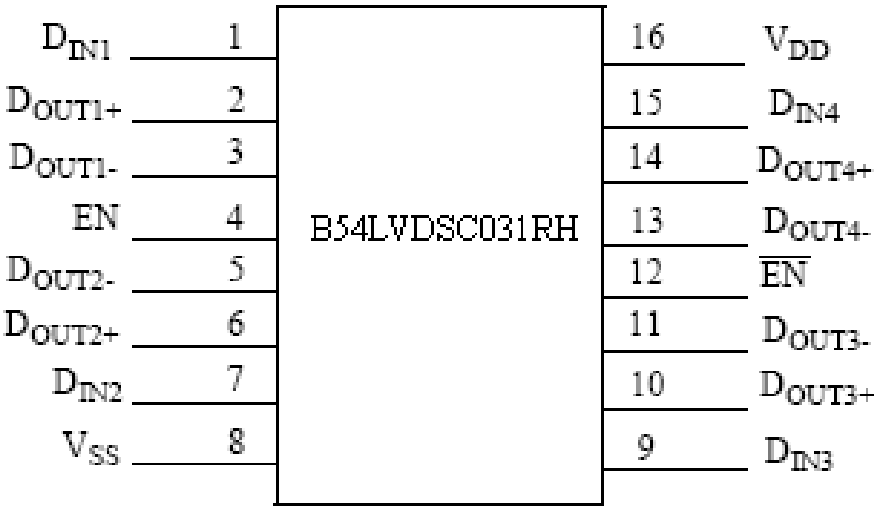


Figure 4-1 B54LVDSC031RH pin configuration

Talble 4-1 B54LVDSC031RH Pin Function Descriptions

Pin No.	Name	Description
1，7，9，15	D_{IN}	Driver input pin, TTL/CMOS compatible
2，6，10，14	D_{OUT+}	Non-inverting driver output pin, LVDS levels
3，5，11，13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN
12	$\overline{EN}$	Active low enable pin, OR-ed with EN
16	V_{DD}	Power supply pin, +5V + 10%
8	V_{SS}	Ground pin

5. Pin List

B54LVDSC031RH –pin list is shown in table 5-1.

Table 5-1 B54LVDSC031RH – pin list

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	D_{IN1}	INPUT DATA1	9	D_{IN3}	INPUT DATA3
2	D_{OUT1+}	OUTPUT DATA1 POSITIVE	10	D_{OUT3+}	OUTPUT DATA3 POSITIVE
3	D_{OUT1-}	OUTPUT DATA1 NEGATIVE	11	D_{OUT3-}	OUTPUT DATA3 NEGATIVE
4	EN	Active high enable pin	12	$\overline{EN}$	Active low enable pin
5	D_{OUT2-}	OUTPUT DATA2 NEGATIVE	13	D_{OUT4-}	OUTPUT DATA4 NEGATIVE
6	D_{OUT2+}	OUTPUT DATA2 POSITIVE	14	D_{OUT4+}	OUTPUT DATA4 POSITIVE
7	D_{IN2}	INPUT DATA2	15	D_{IN4}	INPUT DATA4
8	V_{SS}	GND	16	V_{DD}	POWER

6. Detailed Description

6.1 Function Description

The device is designed to support data rates in excess of 155.5 Mbps(77.7 MHz) utilizing Low Voltage Differential Signaling(LVDS) technology. The B54LVDSC031RH accepts TTL input levels and translates them to low voltage (340mV) differential output signals. In addition, the driver supports a three-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state. truth table is shown in table 6-1.

Table 6-1 truth table

ENABLE	$\overline{ENABLE}$	Input	Non-inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

L = Low logic state

X = Irrelevant

H = High logic state

Z = TRI-STATE (high impedance)

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment,

6.3 Absolute Maximum Ratings

a) Supply voltage range to ground potential（V_{DD}）： -0.3V to 6.0 V
b) DC input voltage range（V_{in}）： -0.3V to（V_{DD}+0.3V）
c) Storage temperature（T_{stg}）： -65℃ to 150℃
d) Lead temperature（T_h）： 260℃
e) Junction temperature (TJ)： 150℃
f) Thermal resistance junction-to-case3 ($R_{th(J-C)}$)： 20℃/W

6.4 Recommended Operation Conditions

a) Supply voltage relative to ground（V_{DD}）： 4.5 V ~ 5.5 V
b) Case operation temperature range(TA)： -55℃ to 125℃
c) DC input voltage (V_I)： 0V to V_{DD}

7. Specifications

All electrical characteristics are shown in table 7-1，Propagation Delay and Transition Time Waveforms are shown in Figure 7-1，Three-State Delay Waveform is shown in Figure 7-2.

Table 7-1 B54LVDSC031RH electrical characteristics

PARAMETER	SYMBOL	CONDITION	LIMIT		UNIT
		（-55℃≤ T_A ≤ 125℃ ， V_{DD}=5.0×（1±10%）V）	MIN	MAX	
High-level input voltage	V_{IH}		2.0	V_{DD}	V
Low-level input voltage	V_{IL}		GND	0.8	V
High-level output voltage	V_{OH}	R_L=100Ω	—	1.6	V
Low-level output voltage	V_{OL}	R_L=100Ω	0.9	—	V
Input leakage current	I_{IN}	V_{IN}= V_{DD}orV_{SS}， V_{DD}=5.5V	-10	10	μA
Cold spare current	I_{CS}	V_{OUT}=5.5V， V_{DD}=0V	-10	10	μA
Differential Output Voltage	V_{OD}	R_L=100Ω	250	400	mV
Change in Magnitude of VOD for Complementary Output States	$\triangle V_{OD}$	R_L=100Ω	—	10	mV
Offset Voltage	V_{OS}	R_L=100Ω， V_{OS} =(V_{OL}+V_{OH}) /2	1.125	1.375	V
Change in Magnitude of VOS for Complementary Output States	$\triangle V_{OS}$	R_L=100Ω	—	25	mV
Input clamp voltage	V_{CL}	I_{CL} =-18 mA	-1.5	—	V
Output Short Circuit Current[a]	I_{OS}	V_{IN}=V_{DD},V_{OUT+}=0V 或 V_{IN}=0V,V_{OUT-}=0V	-5.0	—	mA
Output Three-State Current	I_{OZ}	V_{DD}=5.5V, EN=0V， $\overline{EN}$ =5.5V， V_{OUT-}=0V or V_{DD}	-10	10	μA
Loaded supply current drivers enabled	I_{CCL}	RL = 100Ω all channels V_{IN} = V_{DD} or V_{SS} (all inputs)	—	25.0	mA
Loaded supply current drivers disabled	I_{CCZ}	EN=0V， $\overline{EN}$ =V_{DD}， V_{IN}= V_{DD} or 0V	—	10	mA
Function test		f =77.7MHz			
Differential Propagation Delay High to Low	t_{PHLD}	Figure 7-1	—	5.0	ns
Differential Propagation Delay Low to High	t_{PLHD}	Figure 7-1	—	5.0	ns

Differential Skew (tPHLD - tPLHD)	t_{SKD}	t_{PLHD} -t_{PHLD}	—	3.0	ns
Channel-to-Channel Skew[b]	t_{SK1}		—	3.0	ns
Chip-to-Chip Skew[c]	t_{SK2}		—	4.5	ns
Rise Time	t_{TLH}	Figure 7-1		2.0	ns
Fall Time	t_{THL}	Figure 7-1		2.0	ns
Disable Time High to Z	t_{PHZ}	Figure 7-2	—	10	ns
Disable Time Low to Z	t_{PLZ}	Figure 7-2	—	10	ns
Enable Time Z to High	t_{PZH}	Figure 7-2	—	10	ns
Enable Time Z to Low	t_{PZL}	Figure 7-2	—	10	ns

Notes：

1、Devices are tested Devices are tested @ VDD = 4.5V&5.5V.

2、Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.

3、Generator waveform for all tests unless otherwise specified: f = 1 MHz, ZO = 50Ω, tr < 6 ns, and tf < 6 ns.

[a] Output short circuit current (IOS) is specified as magnitude only, minus sign indicates direction only.

[b] Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.

[c] Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

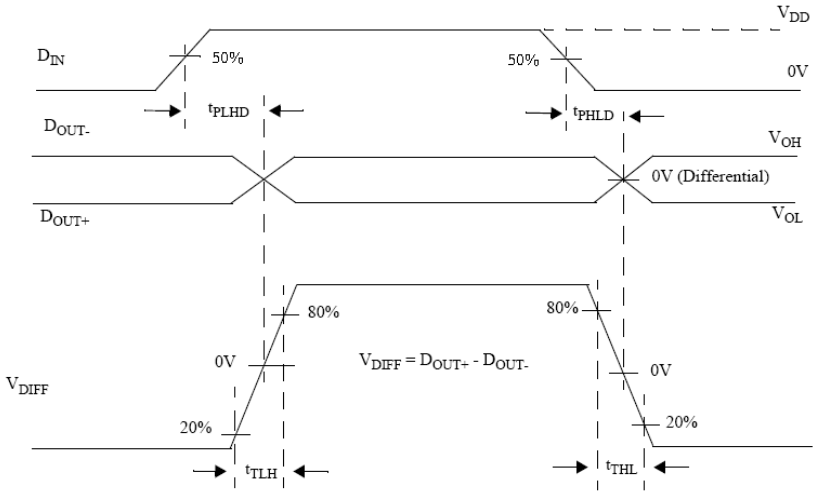


Figure.7-1. Driver Propagation Delay and Transition Time Waveforms

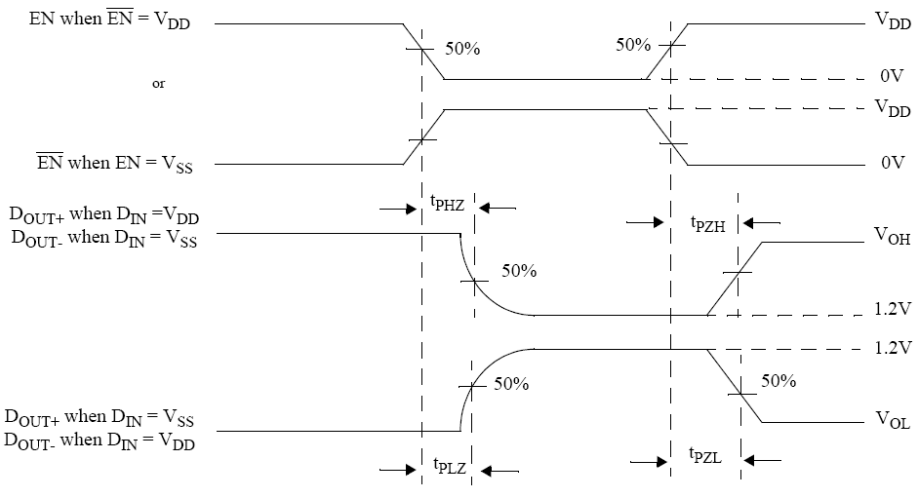


Figure.7-2. Driver Three-State Delay Waveform

8. Package Specifications

B54LVDSC031RH adopt 16-Lead Ceramic Quad Flat package, as in Figure 8-1 and the size is listed in Table 8-1.

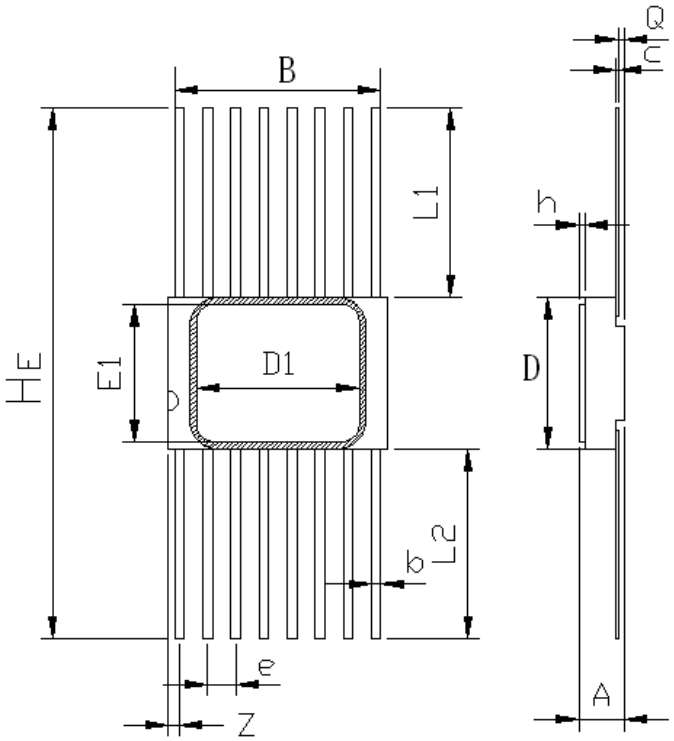


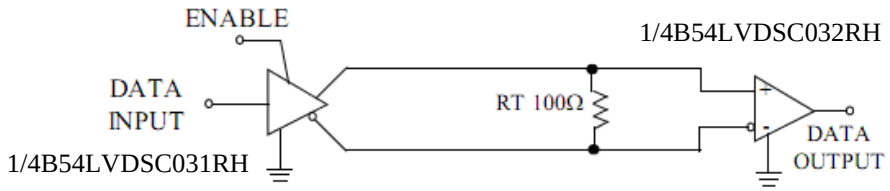
Figure 8-1 Flat Package Outline

Table 8-1 Flat Package Size

Symbol	Value（unit：mm）		
	Min	Normal	Max
A	1.60	——	2.50
B	8.94	——	9.69
b	0.25	——	0.54
c	0.07	——	0.20
D	6.55	——	7.25
e	——	1.27	——
He	18.76	19.41	20.06
Q	0.13	——	0.90
L1	5.75	——	6.75
L2	5.75	——	6.75
Z	——	——	1.27
D1	——	7.366	——
E1	——	6.223	——
h	0.22	——	0.28

9. Appendix I Typical Application Example

The B54LVDSC031RH driver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Appendix figure.1-1. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media such as a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into voltages that are detected by the receiver. Other configurations are possible such as a multireceiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities, as well as ground shifting, noise margin limits, and total termination loading must be taken into account.



Appendix figure.1-1. Point-to-Point Application

The B54LVDSC031RH differential line driver is a balanced current source design. A current mode driver, has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The current mode requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Appendix figure.1-1. AC or unterminated configurations are not allowed. The 3.5mA loop current will develop a differential voltage of 350mV across the 100Ω termination resistor which the receiver detects with a 250mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350mV - 100mV = 250mV)). The signal is centered around +1.125V (Driver Offset, VOS) with respect to ground.

10. Appendix II Replaced Product

Appendix table1-1

Device Type	Substituted Device Type
B54LVDSC031RH	Aeroflex UT54LVDSC031

Service and Support：

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