Ver 1.2

Radiation-Hardened SRAM

Datasheet

Part Number：B8R512K8RH

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Page of Revise Control

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1. Features

- 15 ns maximum access time
- Asynchronous operation, functionally compatible with Aeroflex UT8R512K8 SRAM
- CMOS compatible inputs and output levels, three-state bidirectional data bus
- I/O Voltage 3.3 V， 1.8 V core
- ESD better than 2000 V
- Operational environment:
  Total-dose: 100 K Rad (Si)
  SEL Immune> 75 MeV cm^2/mg
  SEU Error Rate:1E-10errors/bit day in Geosynchronous Orbit
- Packaging options
  36-lead ceramic flatpack（CFP36）

2. General Description

The B8R512K8RH is a high-performance radiation-hardened CMOS static RAM organized as 524,288 words by 8 bits. Fabricated with industry-standard CMOS technology, the device works in asynchronous mode and is functionally compatible with Aeroflex UT8R512K8. Featuring fully static operation, the B8R512K8RH requires no external clocks. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. The combination of radiation-hardness, fast access time, and low power consumption makes the B8R512K8RH ideal for high speed system designed for operation in radiation environments.

3. Block Diagram

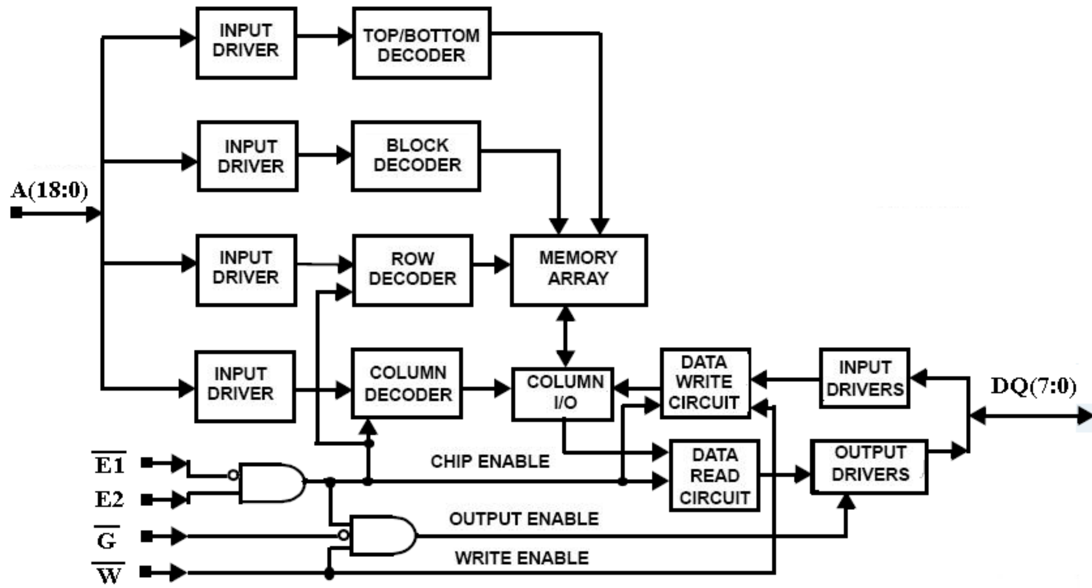


Figure 1. B8R512K8RH Block Diagram

4. Pin Description

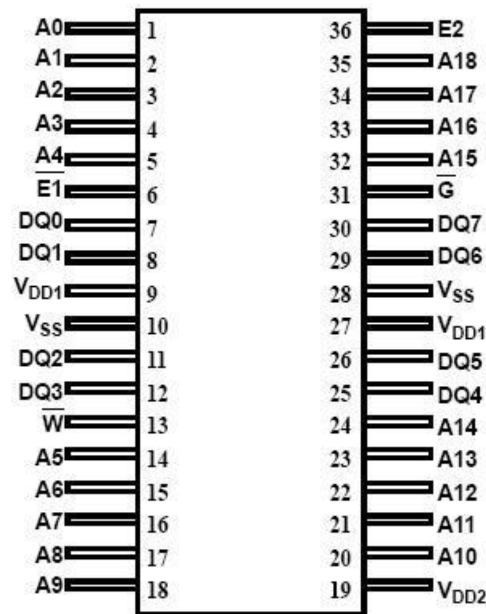


Figure 2. B8R512K8RH SRAM Pinout (36)

Table 1. Pin Names

Pin Names	Functions
A0~A18	Address
DQ0~DQ7	Data Input / Output
$\overline{E1}$	Chip Enable 1 (Active Low)
E2	Chip Enable 2 (Active High)
$\overline{W}$	Write Enable (Low Write Enable, and High Read Enable)
$\overline{G}$	Output Enable (Active Low)
VDD1	Power (1.8 V)
VDD2	Power (3.3 V)
VSS	Ground
NC	No Connect

5. Pin Configurations（Appendix 1）

6. Product Description

6.1 Quality Grade and Production Standard

The quality grade of the radiation-hardened SRAM B8R512K8RH is GJB597A-1996 B. And B8R512K8RH is up to the Q/Zt 20198-2011 semiconductor IC standard and CASTPSW11/337-2011 standard.

6.2 Function Description

The B8R512K8RH has four control inputs called Chip Enable 1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$), 19 address inputs A (18:0), and 8 bidirectional data lines, DQ (7:0).

Table 2. Device Operation Truth Table

Inputs				Outputs	
$\overline{G}$	**$\overline{W}$**	**E2**	**$\overline{E1}$**	**I/O Mode**	**Mode**
X	X	X	1	DQ(7:0) 3-State	Standby
X	X	0	X	DQ(7:0) 3-State	Standby
0	1	1	0	DQ(7:0) Data out	Read
X	0	1	0	DQ(7:0) Data in	Write
1	1	1	0	DQ(7:0) 3-State	Read DQ 3-State

Notes:

1. X = Don't care

◆ Read Cycle

A combination of $\overline{W}$ and E2 greater than V_{IH}(min) and $\overline{E1}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 4, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ (7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enables and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5, is initiated by the latter of $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted， $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 8-bit word addressed by A (18:0) is accessed and appears at the data outputs DQ (7:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 6, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

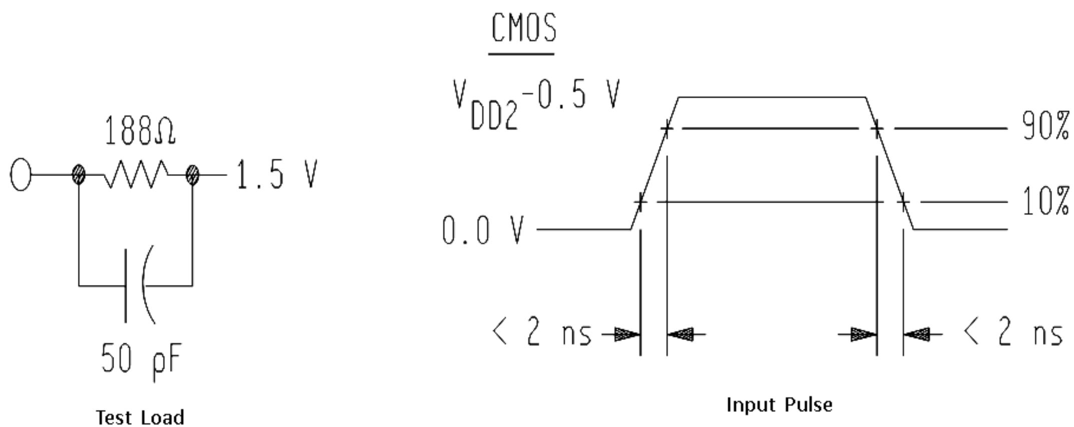
- **Write Cycle**

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL}(max) and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 7, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$ or E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 8 bidirectional pins DQ (7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 8, is defined by a write terminated by either of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by either $\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 8 bidirectional pins DQ (7:0) to avoid bus contention.

6.3 AC Test Load and Input Waveforms



Notes: 1. 50pF includes scope probe and test socket capacitance.

2. Measurement of data output occurs at the low to high or high to low

transition mid-point (i.e., CMOS input = V_{DD2}/ 2).

Figure 3. AC Test Load and Input Waveforms

6.4 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	1.7 V ~ 1.9 V
V_{DD2}	I/O supply voltage	3.0 V ~ 3.6 V
T_C	Case temperature range	-55℃ ~ +125℃
V_I	DC input voltage	0 V ~ V_{DD2}

Notes:

The correct power-up sequence should be V_{DD1}--> V_{DD2}.

7． Electrical Characteristics

7.1 DC Electrical Characteristics (Pre and Post-Radiation)

Table 4. DC Parameter Table (Ⅰ)

Parameter	Symbol	Condition (GND=0V，-55℃≤T_A≤125℃) 1.7V≤V_{DD1}≤1.9V、3.0V≤V_{DD2}≤3.6V	Limits		UNIT
			MIN	MAX	
High-level input voltage	V_{IH}		.7*V_{DD2}	—	V
Low-level input voltage	V_{IL}		—	.3*V_{DD2}	V
High-level output voltage	V_{OH}	V_{DD2}=3V, I_{OH}=-4 mA, all outputs needed are tested	.8*V_{DD2}	—	V
Low-level output voltage	V_{OL}	V_{DD2}=3V, I_{OL}=8 mA, all outputs needed are tested	—	.2*V_{DD2}	V
Input capacitance	C_{IN}[1]	f=1MHz@0V, T_C=25 ℃		12	pF

Bidirectional I/O Capacitance	C_{IO}[1]	f=1MHz@0V, T_C=25 ℃		12	pF
High-level input leakage current	I_{IH}	V_{DD2}=3.6V, V_{DD1}=1.9V, V_I=3.6V, all inputs are tested	-2	2	μA
Low-level input leakage current	$\|I_{IL}\|$	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_I= 0V, all inputs are tested	-2	2	μA
Three-state (high-level) output leakage current	I_{OZH}	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_O=V_{DD2}, all bidirectional I/O are tested	-2	2	μA
Three-state (low-level) output leakage current	$\|I_{OZL}\|$	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_O=0, all bidirectional I/O are tested	-2	2	μA
Core Supply current operating @1MHz	$I_{DD1}(OP_1)$	V_{IL}=0.2V, V_{IH}=3.4V, I_{DD1} current is tested V_{DD1}=1.9V		15	mA

Table 4. DC Parameter Table (Ⅱ)

Parameter	**Symbol**	**Condition** （**GND=0V，-55℃≤T_A≤125℃**） **1.7V≤V_{DD1}≤1.9V、3.0V≤V_{DD2}≤3.6V**	**Limits**		**UNIT**
			MIN	**MAX**	
Core Supply current operating @66MHz	$I_{DD1}(OP_2)$	V_{IL}=0.2V, V_{IH}=3.4V, I_{DD1} current is tested V_{DD1}=1.9V		80	mA
I/O Supply current operating @1 MHz	$I_{DD2}(OP_1)$	V_{IL}=0.2V, V_{IH}=3.4V, V_{DD1}=1.9V, V_{DD2}=3.6V, I_{DD2} current is tested		2	mA
I/O Supply current operating @66 MHz	$I_{DD2}(OP_2)$	V_{IL}=0.2V, V_{IH}=3.4V, V_{DD1}=1.9V, V_{DD2}=3.6V, I_{DD2} current is tested		4	mA
Supply current standby @0 Hz	$I_{DD1}(SB)$	CMOS inputs, I_{OUT}=0，$\overline{E1}$=V_{DD2}-0.2, E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		11	mA

Supply current standby @0 Hz	$I_{DD2}(SB)$	CMOS inputs, I_{OUT}=0， $\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}=3.6V, V_{DD1}=1.9V		100	μA
Supply current standby A (16:0) @66M Hz	$I_{DD1}(SB)$	CMOS inputs,I_{OUT}=0， $\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		11	mA
Supply current standby A (16:0) @66M Hz	$I_{DD2}(SB)$	CMOS inputs,I_{OUT}=0， $\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		100	μA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. V_{IH}=V_{DD2}.

7.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 5. Read Cycle AC Parameters

Parameter	Symbol	Condition (V_{DD1}=V_{DD1}(min), V_{DD2}=V_{DD2}(min), -55℃≤ T_A≤ 125℃)	Limits		UNIT
			MIN	MAX	
Read cycle time	t_{AVAV}[1]	Figure 4	15	—	ns

Address to data valid	t_{AVQV}		—	15	ns
Output hold time from address change	t_{AXQX}[2]		3	—	ns
$\overline{G}$-controlled output enable time	t_{GLQX}[2,1]	Figure 6	0	—	ns
$\overline{G}$-controlled output data valid	t_{GLQV}		—	7	ns
$\overline{G}$-controlled output three-state time	t_{GHQZ}[2]		—	7	ns
$\overline{E1}$-controlled output enable time	t_{ETQX}[2,3]	Figure 5	5	—	ns
$\overline{E1}$-controlled access time	t_{ETQV}[3]		—	15	ns
$\overline{E1}$-controlled output three-state time	t_{EFQZ}[2,4]		—	7	ns

Notes:

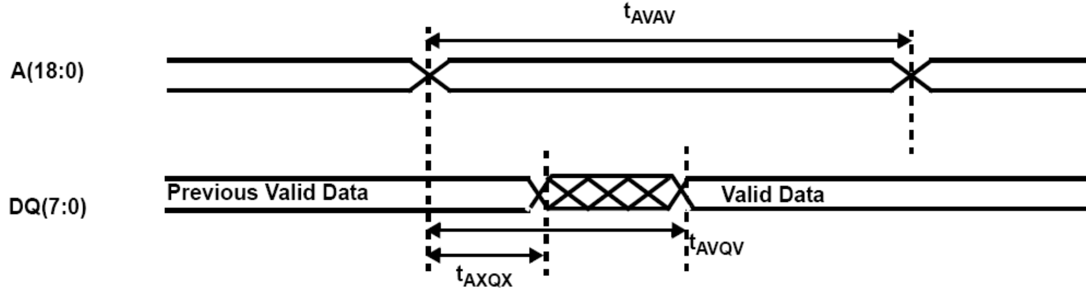
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Guaranteed but not tested.

2. Three-state is defined as a 200mV change from steady-state output voltage.

3. The ET (chip enable true) notation refers to the latter falling edge of $\overline{E1}$ or rising edge of E2.

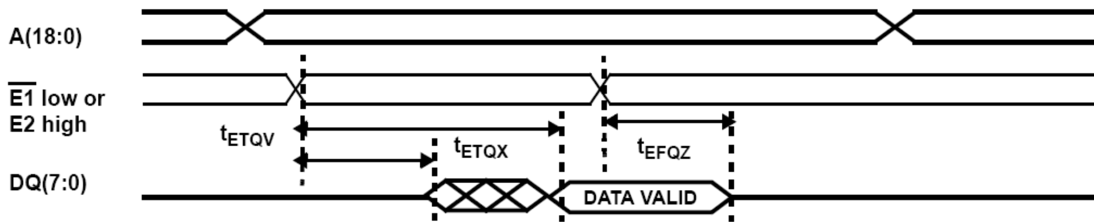
4. The EF (chip enable false) notation refers to the latter rising edge of $\overline{E1}$ or falling edge of E2.



Assumptions:

$\overline{E1} \leq V_{IL}(max)$, $\overline{G} \leq V_{IL}(max)$, $\overline{W} \geq V_{IH}(min)$, $E2 \geq V_{IH}(min)$

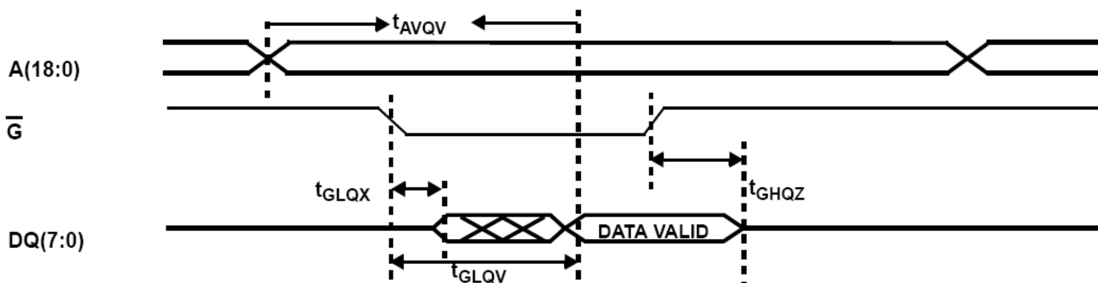
Figure 4. SRAM Read Cycle 1: Address Access



Assumptions：

1. $\overline{G}$, $\overline{HHWE}$, $\overline{LHWE} \leq V_{IL}(max)$, $\overline{W} \geq V_{IH}(min)$
2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 5. SRAM Read Cycle 2: Chip Enable Access



Assumptions:

1. $\overline{E1} \leq V_{IL}(max)$, $\overline{W} \geq V_{IH}(min)$, $E2 \geq V_{IH}(min)$
2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 6. SRAM Read Cycle 3: Output Enable Access

7.3 Write Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 6. Write Cycle AC Parameter

Parameter	Symbol	Condition (V_{DD1}=V_{DD1}(min), V_{DD2}=V_{DD2}(min), -55℃≤T_A≤125℃)	Limits		UNIT
			MIN	MAX	
Write cycle time	t_{AVAV}[1]	Figure 7 & Figure 8	15		ns
Chip enable to end of write	t_{ETWH}	Figure 7	12	—	ns
Address setup time for write ($\overline{E1}$/E2-controlled)	t_{AVET}		0	—	ns
Address setup time for write ($\overline{W}$-controlled)	t_{AVWL}	Figure 7	1	—	ns
Write pulse width	t_{WLWH}	Figure 7	12	—	ns
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}	Figure 7	2	—	ns
Address hold time for chip enable ($\overline{E1}$/E2-controlled)	t_{EFAX}	Figure 8	0	—	ns
$\overline{W}$ -controlled three-state time	t_{WLQZ}[2]	Figure 7	—	5	ns
$\overline{W}$-controlled output enable time	t_{WHQX}[2]	Figure 7	4	—	ns
Chip enable pulse width ($\overline{E1}$/E2-controlled)	t_{ETEF}	Figure 8	12	—	ns
Data setup time	t_{DVWH}	Figure 7	7	—	ns
Data hold time	t_{WHDX}	Figure 7	2	—	ns

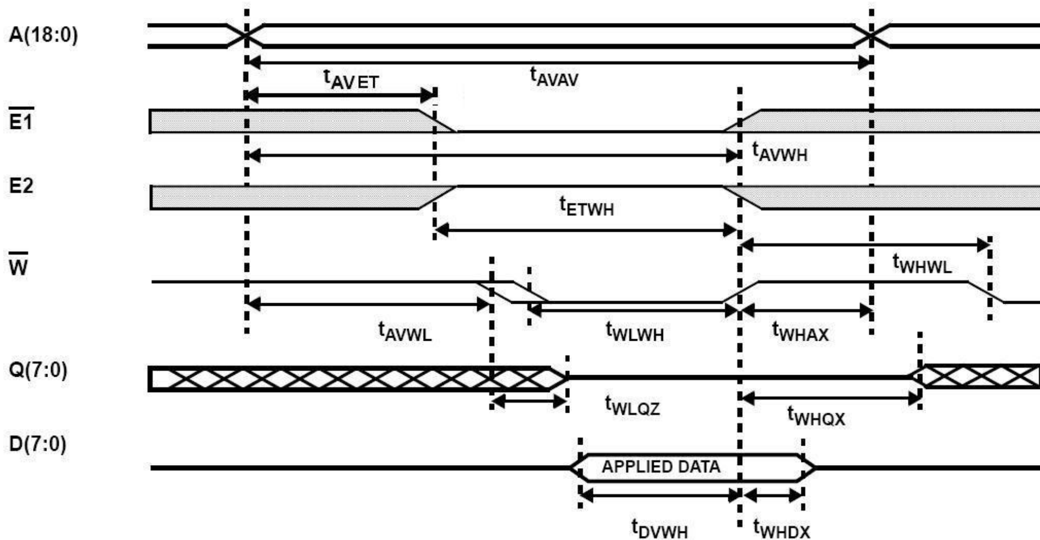
Chip enable controlled write pulse width	t_{WLEF}	Figure 8	12	—	ns
Data setup time	t_{DVEF}	Figure 8	7	—	ns
Data hold time	t_{EFDX}	Figure 8	0	—	ns
Address valid to end of write	t_{AVWH}	Figure 7	12	—	ns
Write disable time	t_{WHWL}[1]	Figure 7	3	—	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Tested with $\overline{G}$ high.

2. Three-state is defined as 200mV change from steady-state output voltage.

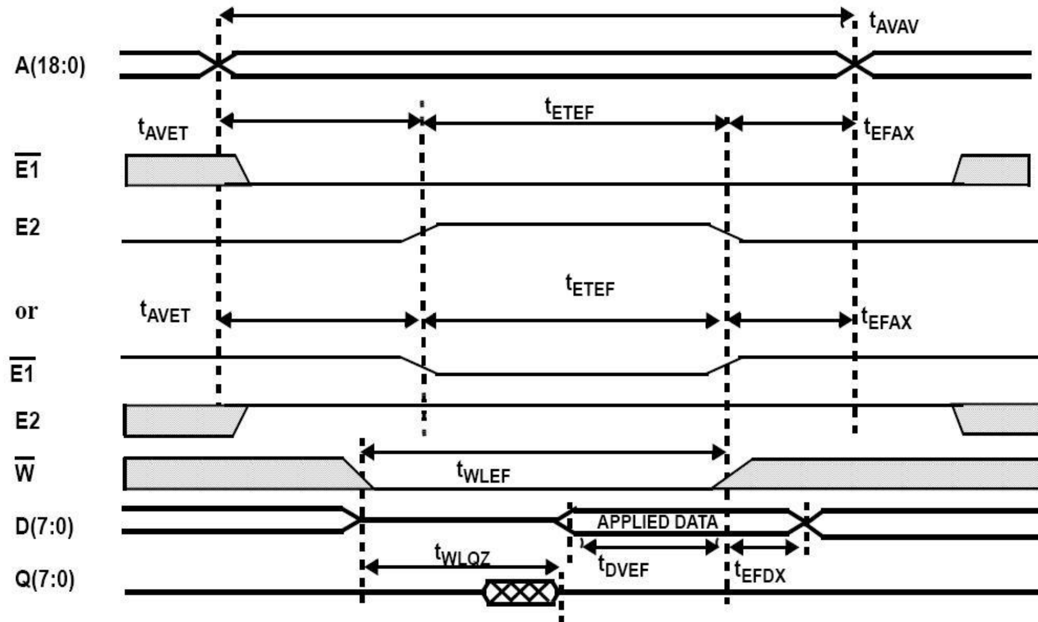


Assumptions:

1. $\overline{G} \le V_{IL}$(max). If $\overline{G} \ge V_{IH}$(min) then Q(8:0) will be in three-state for the entire cycle.

2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 7. SRAM Write Cycle 1: $\overline{W}$-controlled Access



Assumption:

1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$(min) then Q(8:0) will be in three-state for the entire cycle.

2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 8. SRAM Write Cycle 2: Enable-chip Controlled Access

7.4 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

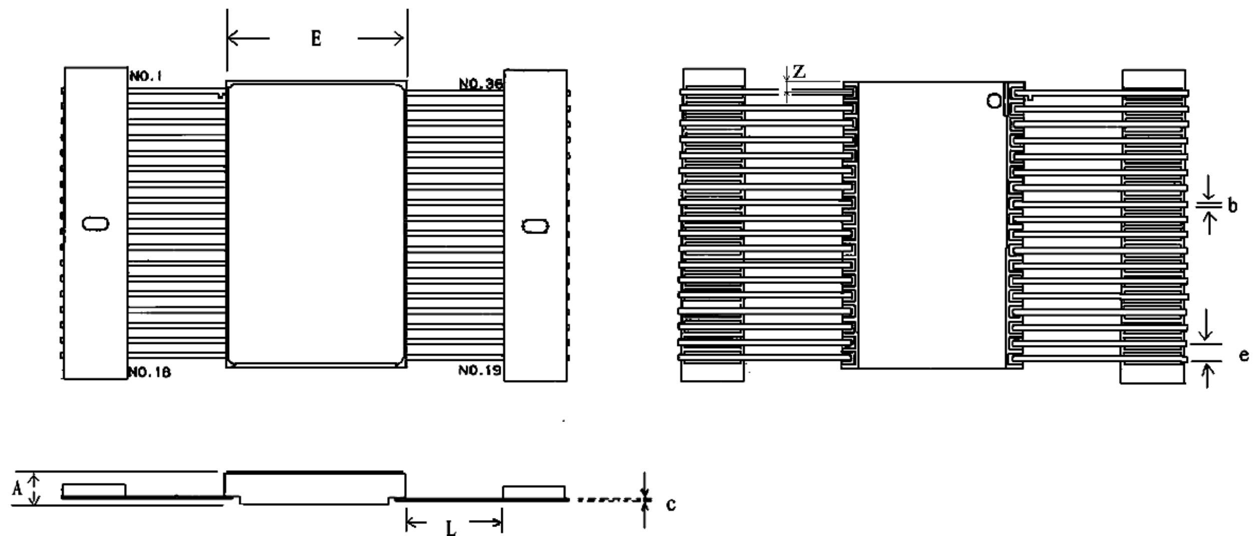
Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	-0.3V ~ +2.1 V
V_{DD2}	I/O supply voltage	-0.3V ~ +3.8 V
$V_{I/O}$	Voltage on any pin	-0.3V ~ +3.8 V
T_{STG}	Storage Temperature	-65℃ ~ 150℃
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature	+175℃

$R_{th(J-C)}$	Thermal resistance, junction-to-case	5℃/W

8. Typical Application（Appendix 2）

9. Packaging

The SRAM B8R512K8RH utilizes 36-Lead Ceramic Flatpack as shown in Figure 9 and the corresponding dimensions are listed in Table 8, which is accordance with GB/T7092.



Notes:

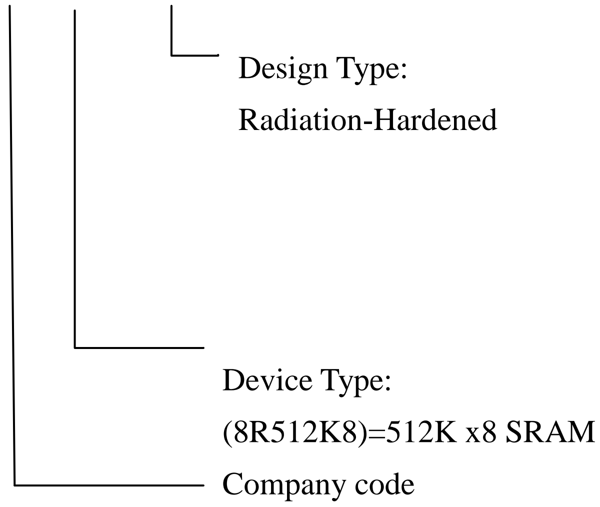
1. The lid is electrically connected to V_{SS}.

Figure 9. Package Outline

Table 8. Package Dimensions

Symbol	Value (Unit: mm)		
	Min	Normal	Max
A	—	—	3.4
b	0.35	—	0.51
c	0.07	—	0.22
e	—	1.27	—
L	7.5	—	8.5
E	14	—	15.5
Z	—	—	1.27

10. Naming Rule



Appendix 1

Pin Descriptions are listed in Table 9：

Table 9. Pin Symbols and Functions

Pin NO.	Symbol	Functions	Pin NO.	Symbol	Functions
1	A0	Address	19	V_{DD2}	Power(3.3V)
2	A1	Address	20	A10	Address
3	A2	Address	21	A11	Address
4	A3	Address	22	A12	Address
5	A4	Address	23	A13	Address
6	$\overline{E1}$	Chip Enable 1	24	A14	Address
7	DQ0	I/O	25	DQ4	I/O
8	DQ1	I/O	26	DQ5	I/O
9	V_{DD1}	Power(1.8V)	27	V_{DD1}	Power(1.8V)
10	V_{SS}	Ground	28	V_{SS}	Ground
11	DQ2	I/O	29	DQ6	I/O
12	DQ3	I/O	30	DQ7	I/O
13	$\overline{W}$	Write Enable	31	$\overline{G}$	Output Enable
14	A5	Address	32	A15	Address
15	A6	Address	33	A16	Address
16	A7	Address	34	A17	Address
17	A8	Address	35	A18	Address
18	A9	Address	36	E2	Chip Enable 2

Appendix 2

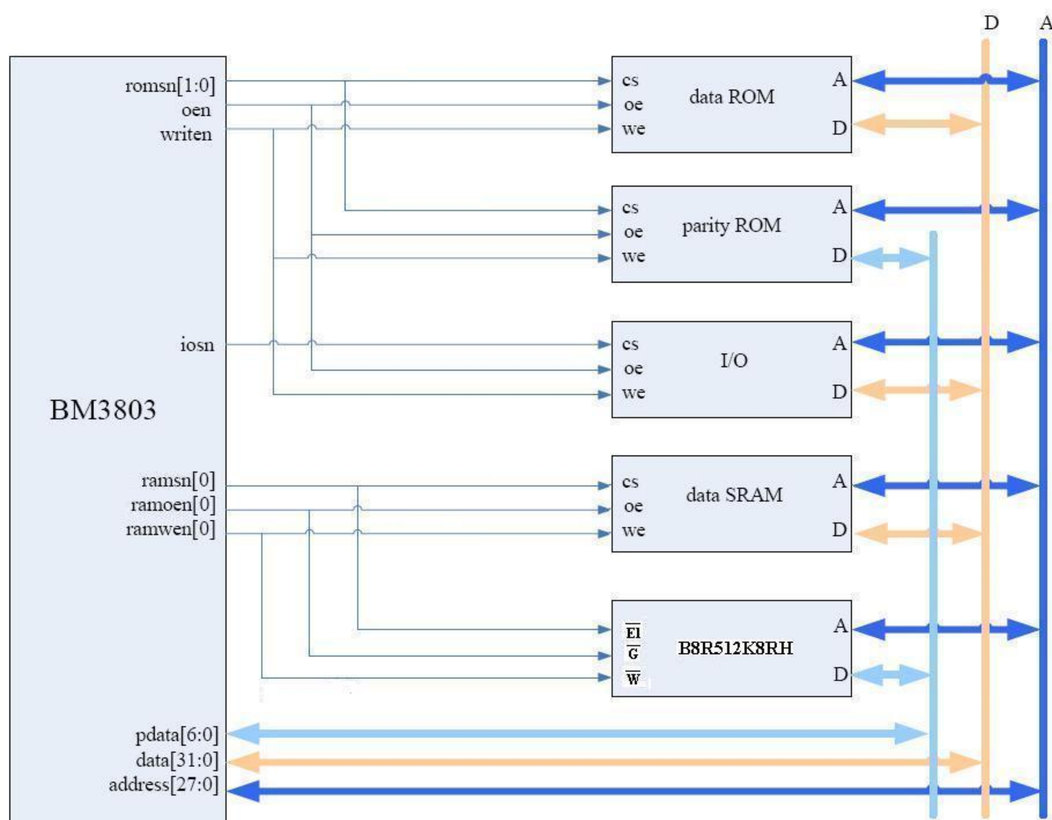


Figure 10. Typical Application

Figure 10 illustrates a typical application system, which consists of a CPU(BM3803) and an SRAM (B8R512K8RH) chip. The B8R512K8RH serves as a parity check memory. The CPU is configured in standard mode for memory accessed. Besides address and data, the main signal include Chip Enable(RAMSN)、Output Enable(RAMOEN) and Write Enable(RWEN).

The access timing is fixed for CPU. Figure 11 discusses read timing and write timing. Base on the access timing of the SRAM(Fig4~Fig8), one should properly configure the control signal .

Notes:

1. Supply voltage sequencing is recommended to be V_{DD2} prior to V_{DD1}.
2. Supply voltage is required to be as stable as possible.
3. The input should not be suspend in midair.

4. The output should not be connected to supply voltage or V_{SS}.
5. The lid is electrically connected to V_{SS}.

There are varied processor in different application, the access timing of SRAM will be different. Such condition requires the system designer to consider the timing carefully.

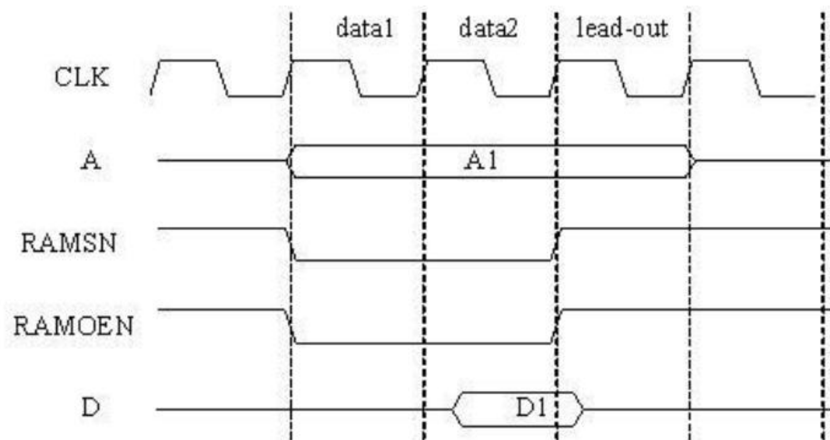


Figure 11（a）Memory read timing of the BM3803

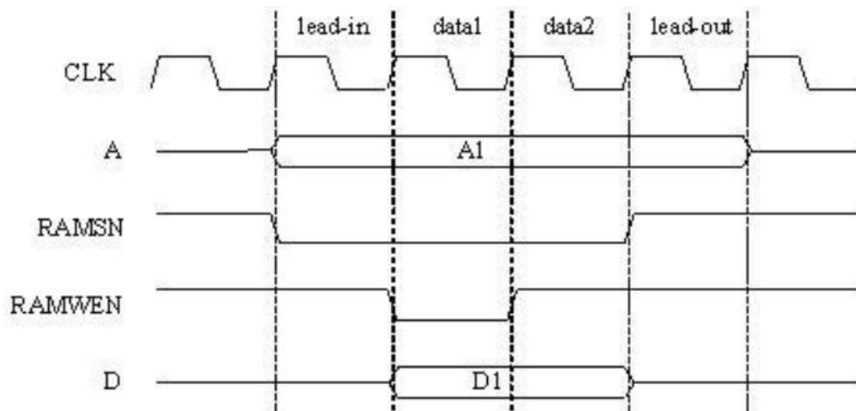


Figure 11（b）Memory write timing of the BM3803

Service & Supply

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