Ver 1.2

Radiation-Hardened SRAM

Datasheet

Part Number：B65608EARH

中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

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1.0	11.25.2012		Document creation	
1.1	07.22.2015	Appendix 2	Advance typical application	
1.2	03.06.2018		Text and wording modifications	

TABLE OF CONTENTS

1. Features

- 45 ns maximum access time
- Asynchronous operation, functional compatible with ATMEL M65608E
- TTL compatible inputs and output levels, three-state bidirectional data bus
- Operating Voltage 5 V
- ESD better than 2000 V
- Operational environment:
  Total-dose: 1000 Gy (Si)
  SEL Immune: > 75 MeV cm^2/mg
  SEU Error Rate=1E-10errors/bit-day in Geosynchronous Orbit
- Packaging options:
  68-lead ceramic quad flatpack（QFP68）

2. General Description

The B65608EARH is a high-performance radiation-hardened asynchronous CMOS static RAM organized as 131,072 words by 8 bits. Fabricated with industry-standard CMOS technology, the device is essentially compatible with ATMEL M65608E and requires no external clocks. The combination of radiation-hardness, fast access time, and low power consumption makes the B65608EARH ideal for high speed system designed for operation in radiation environments.

3. Block Diagram

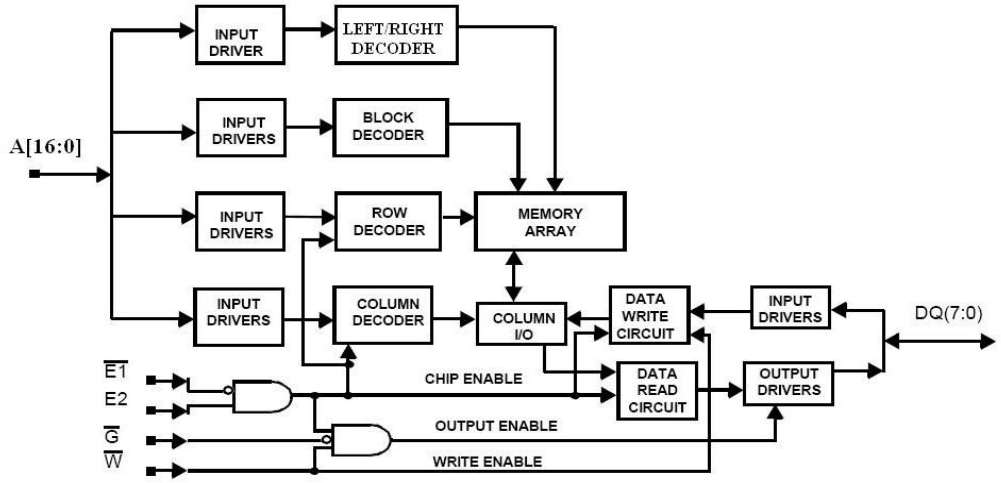


Figure 1. B65608EARH Block Diagram

4. Pin Description

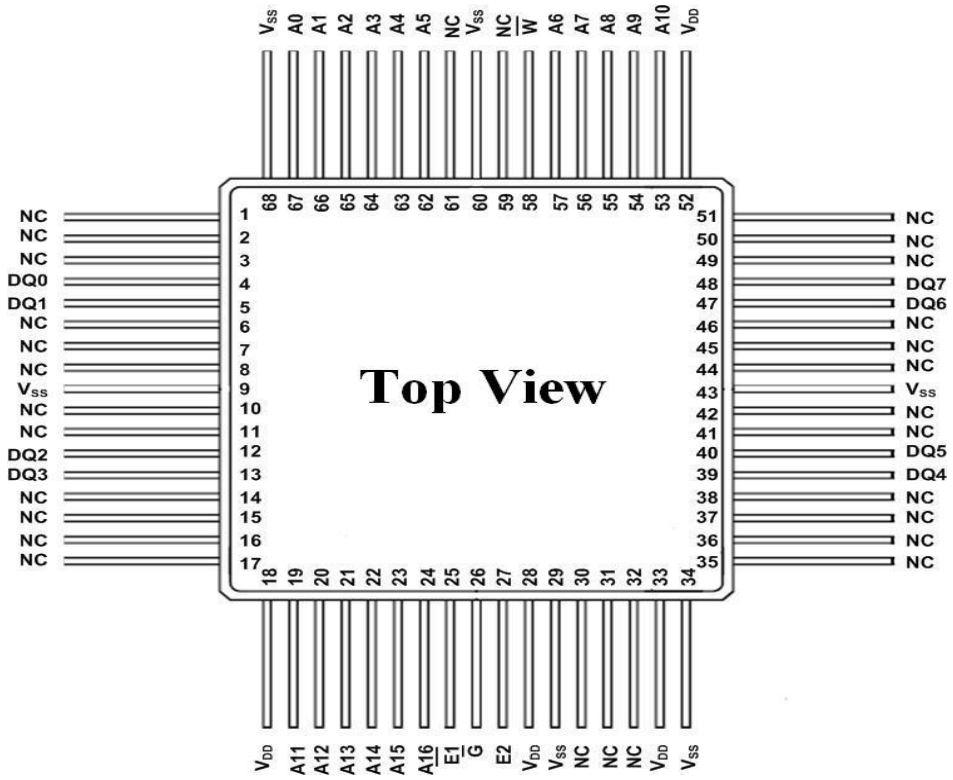


Figure 2. B65608EARH SRAM Pinout (68)

Table 1. Pin Names

Pin Names	Functions
A0~A16	Address
DQ0~DQ7	Data Input / Output
$\overline{E1}$	Chip Enable 1 (Active Low)
E2	Chip Enable 2 (Active High)
$\overline{W}$	Write Enable (Low Write Enable, and High Read Enable)
$\overline{G}$	Output Enable (Active Low)
VDD	Power (5 V)
VSS	Ground
NC	No Connect

5. Pin Configurations（Appendix 1）

6. Product Description

6.1 Quality Grade and Production Standard

The quality grade of the radiation-hardened SRAM B65608EARH is GJB597A-1996 B. And B65608EARH is up to the Q/Zt 20157-2011 semiconductor IC standard and CASTPSW11/333-2011 standard.

6.2 Function Description

The B65608EARH has four control inputs called Chip Enable 1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 17 address inputs A (16:0); and 8 bidirectional data lines, DQ (7:0).

Table 2. Device Operation Truth Table

Inputs				Outputs	
$\overline{G}$	$\overline{W}$	$\overline{E1}$	E2	I/O Mode	Mode
X	X	1	X	DQ(7:0) 3-State	Standby
X	X	X	0	DQ(7:0) 3-State	Standby
X	0	0	1	DQ(7:0) Data in	Write
1	1	0	1	DQ(7:0) 3-state	Read
0	1	0	1	DQ(7:0) Data out	Read

Notes:

1. X = Don't care

◆ Read Cycle

A combination of $\overline{W}$ and E2 greater than V_{IH}(min) and $\overline{E1}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 4, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ (7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enables and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5, is initiated by $\overline{E1}$ going active while $\overline{G}$ remains asserted，$\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 8-bit word addressed by A (16:0) is accessed and appears at the data outputs DQ (7:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 6, is initiated by $\overline{G}$ going active while $\overline{E1}$ are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

◆ Write Cycle

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL}(max) and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs

are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 7, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 8 bidirectional pins DQ (7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 8, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by

$\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 8 bidirectional pins DQ (7:0) to avoid bus contention.

6.3 AC Test Load and Input Waveforms

AC Test Conditions

Input Pulse Levels……..GND to 3.0v
Input Rise/Fall Times……..5ns
Input Timing Reference Levels…….1.5V
Output loading IOL/IOH (see figures below)+30 pF

AC Test Loads Waveforms

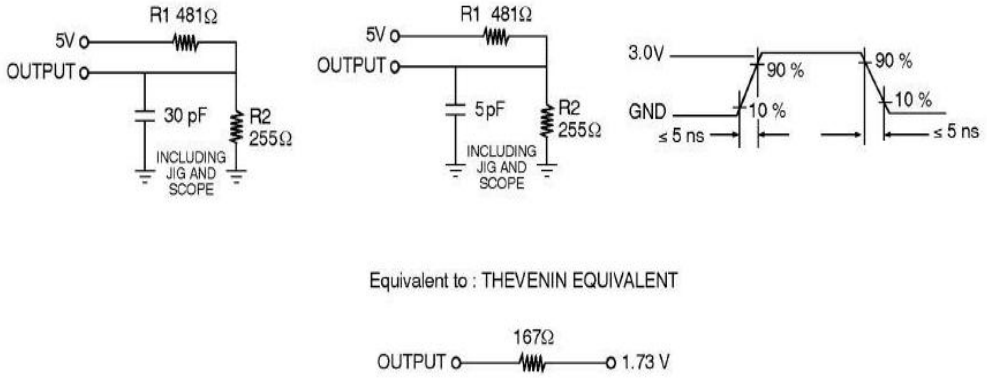


Figure 3. AC Test Loads and Waveforms

6.4 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD}	Supply voltage	4.5 V ~ 5.5 V
V_I	Input voltage	0V ~ V_{DD}
T_C	Case temperature range	-55℃ ~ +125℃

7. Electrical Characteristics

7.1 DC Electrical Characteristics (Pre and Post-Radiation)

Table 4. DC Parameter Table

Parameter	**Symbol**	**Condition** (-55℃≤T_A≤125℃, V_{DD}=5×(1±10%) V)	**Limits**		**UNIT**
			MIN	**MAX**	
High-level input voltage	V_{IH}	TTL，V_{DD}= 5V	2.2	—	V
Low-level input voltage	V_{IL}	TTL，V_{DD}= 5V	—	0.8	V

High-level output voltage	V_{OH}	V_{DD}=4.5V, I_{OH}=-4 mA	2.4	—	V
Low-level output voltage	V_{OL}	V_{DD}=4.5V, I_{OL}=8 mA	—	0.4	V
Input Leakage current	I_{IN}	V_{IN} = V_{DD} or V_{SS}	-1	1	μA
Three-state output leakage current	I_{OZ}	V_O=V_{DD} or V_{SS}，V_{DD}=5.5V，$\overline{G}$ =5.5V	-1	1	μA
Supply current operating @22MHz	I_{DD}(OP)	I_{OUT}=0，V_{DD}=5.5V ，$\overline{W}$ = $\overline{G}$ = V_{IH} ，Vin=Vss or V_{DD}	—	180	mA
Standby Current	I_{DD}(SB)	V_{DD}=5.5V， $\overline{E1}$≥ V_{IH} or E2≤V_{IL}	—	2	mA
Input capacitance	C_{IN}[1]	f=1MHz, T_A=25℃	—	12	pF
Bidirectional I/O Capacitance	C_{IO}[1]	f=1MHz, T_A=25℃	—	12	pF

Notes:

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.

7.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 5. Read Cycle AC Parameters

Parameter	**Symbol**	**Condition** V_{DD}=5×(1±10%) V -55℃ ≤ T_A ≤ 125℃	**Limits**		**UNIT**
			MIN	**MAX**	
Read cycle time	t_{AVAV}	Figure 4 Figure 5 Figure 6	45	—	ns
Address access time	t_{AVQV}		—	45	ns
Address valid to low Z	t_{AVQX}		5	—	ns

$\overline{G}$-controlled output enable time	t_{GLQX}[1]	V_{DD}=4. 5V	0	—	ns
$\overline{G}$-controlled output data valid	t_{GLQV}		—	15	ns
$\overline{G}$-controlled output three-state time	t_{GHQZ}[1]		—	15	ns
$\overline{E1}$-controlled output enable time	t_{E1LQX}[1]		3	—	ns
$\overline{E1}$-controlled access time	t_{E1LQV}		—	45	ns
$\overline{E1}$-controlled output three-state time	t_{E1HQZ}[1]		—	20	ns
E2-controlled output enable time	t_{E2HQX}[1]		3	—	ns
E2-controlled access time	t_{E2HQV}		—	45	
E2-controlled output three-state time	t_{E2LQZ}[1]		—	20	

Note: 1.Guaranteed but not tested.

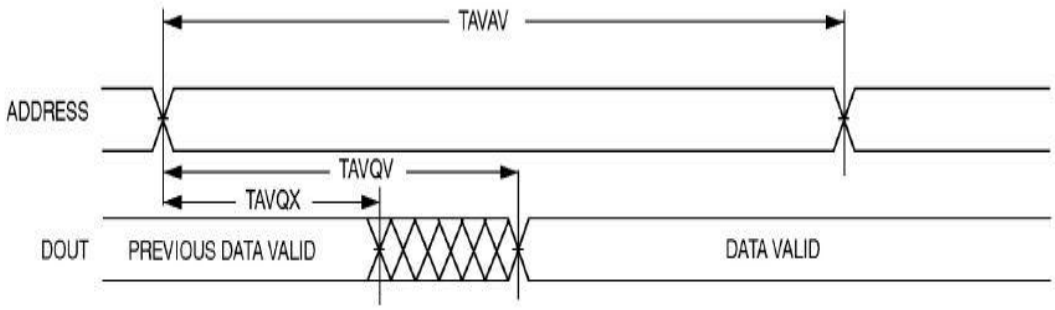


Figure 4. SRAM Read Cycle 1: Address Access

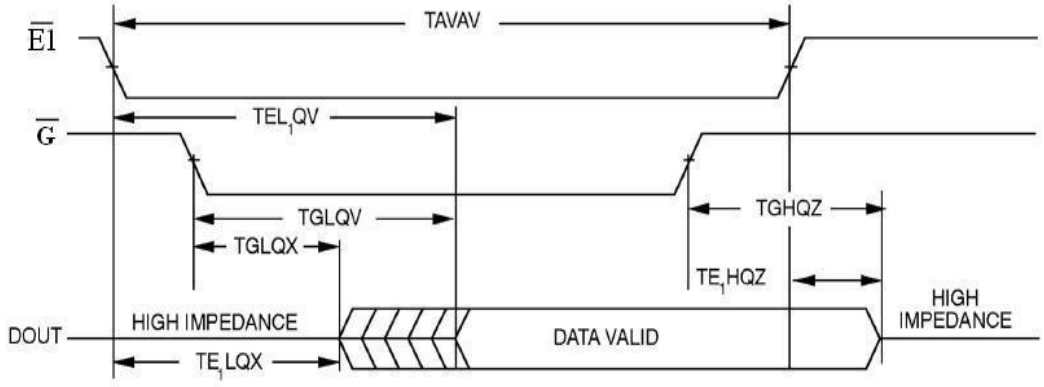


Figure 5. SRAM Read Cycle 2: Chip Enable $\overline{E1}$ Access

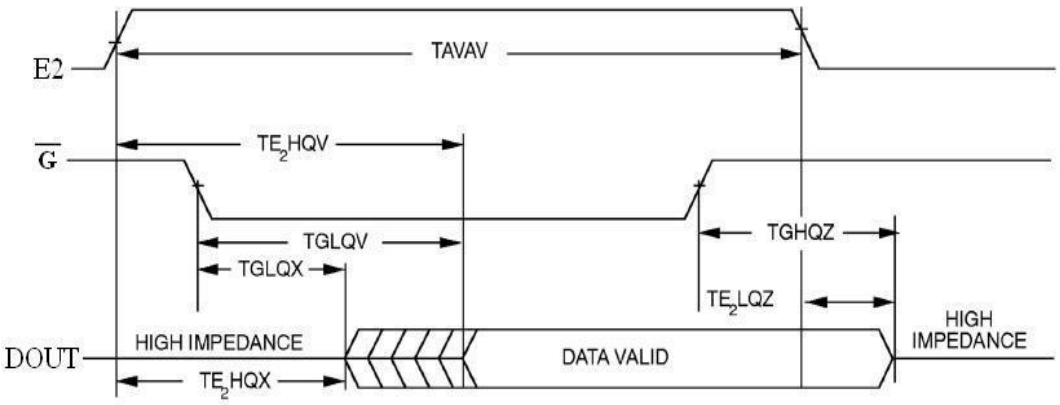


Figure 6. SRAM Read Cycle 3: Output Enable E2 Access

7.3 Write Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 6. Write Cycle AC Parameter

Parameter	Symbol	Condition V_{DD}=5×(1±10%) V -55℃≤T_A≤125℃	Limits		UNIT
			MIN	MAX	
Write cycle time	t_{AVAW}	Figure 7 Figure 8 Figure 9 V_{DD}=4. 5V	45	—	ns
Address valid to end of write	t_{AVWH}		35	—	ns
Address setup time for write ($\overline{W}$-controlled)	t_{AVWL}		3	—	ns
Data setup time	t_{DVWH}		20	—	ns
E1-controlled chip enable to end of write	t_{E1LWH}		35	—	ns
E2-controlled chip enable to end of write	t_{E2HWH}		35	—	ns
$\overline{W}$-controlled three-state time	t_{WLQZ}[1]		—	15	ns
Write pulse width	t_{WLWH}		35	—	ns
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}		0	—	ns
Data hold time	t_{WHDX}		0	—	ns
$\overline{W}$-controlled output enable time	t_{WHQX}[1]		0	—	ns

Notes:

1. Guaranteed but not tested.

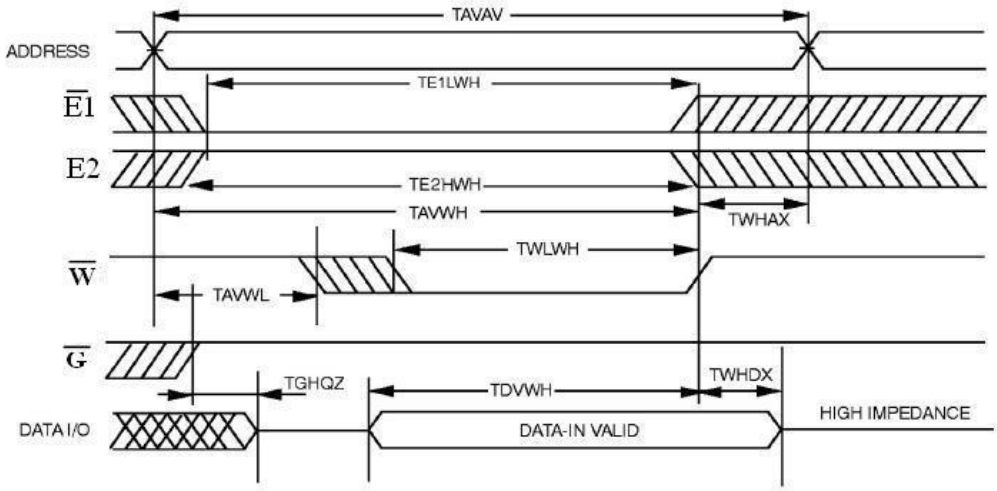


Figure 7. SRAM Write Cycle 1: $\overline{W}$-controlled , $\overline{G}$ high

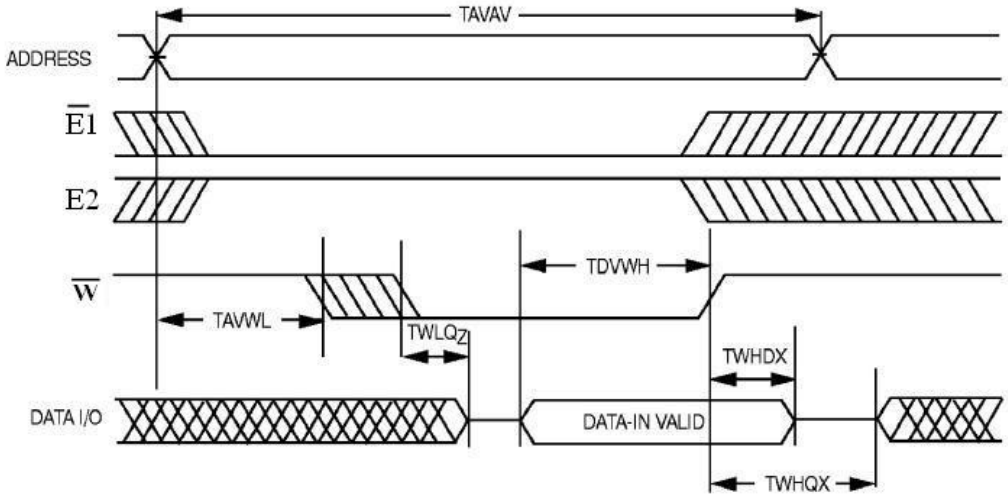


Figure 8. SRAM Write Cycle 2: $\overline{W}$-controlled , $\overline{G}$ low

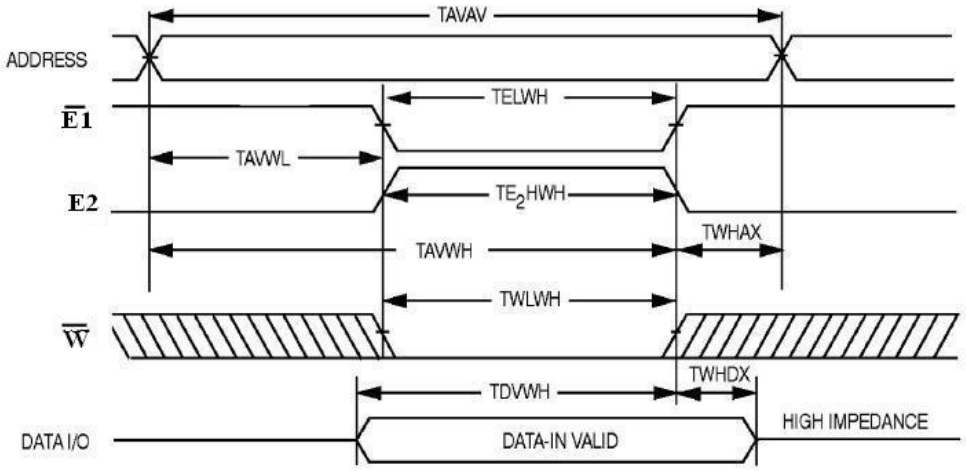


Figure 9. SRAM Write Cycle 3: $\overline{E1}$ or E2 controlled

7.4 Data Retention Characteristics (Pre and Post-Radiation)

Table 7. Data Retention Characteristics

Symbol	Parameter	Minimum	Typical TA=25℃	Maximum	Unit
VCCDR	VCC for data retention	2.0	—	—	V
TCDR	Chip deselect to data retention time	0.0	—	—	ns
TR	Operating recovery time	TAVAV(1)	—	—	ns
ICCDR1	Data retention current at 2.0V	—	0.1	150	μA
ICCDR2(2)	Data retention current at 3.0V	—	0.2	200	μA

Notes:

1. TAVAV=Read Cycle Time
2. $\overline{E1}$=V_{DD2} or E2= $\overline{E1}$=GND, V_{in} =GND/ V_{DD} , this parameter is only tested at $V_{DD=}$2V.
3. Parameters guaranteed but not tested.

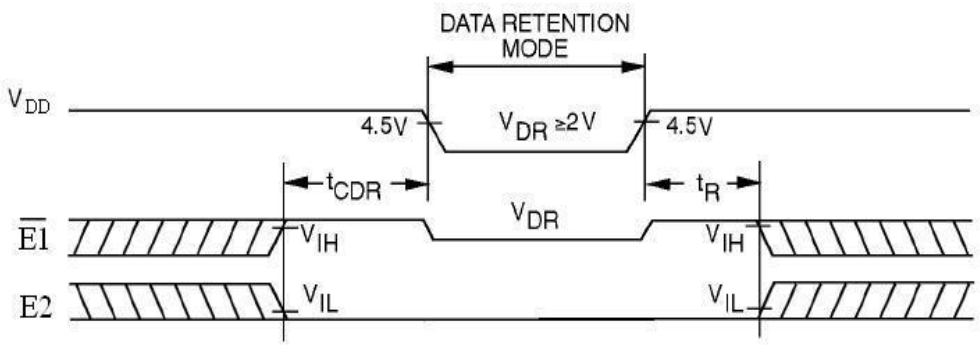


Figure 10. Data Retention Waveform

7.5 Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

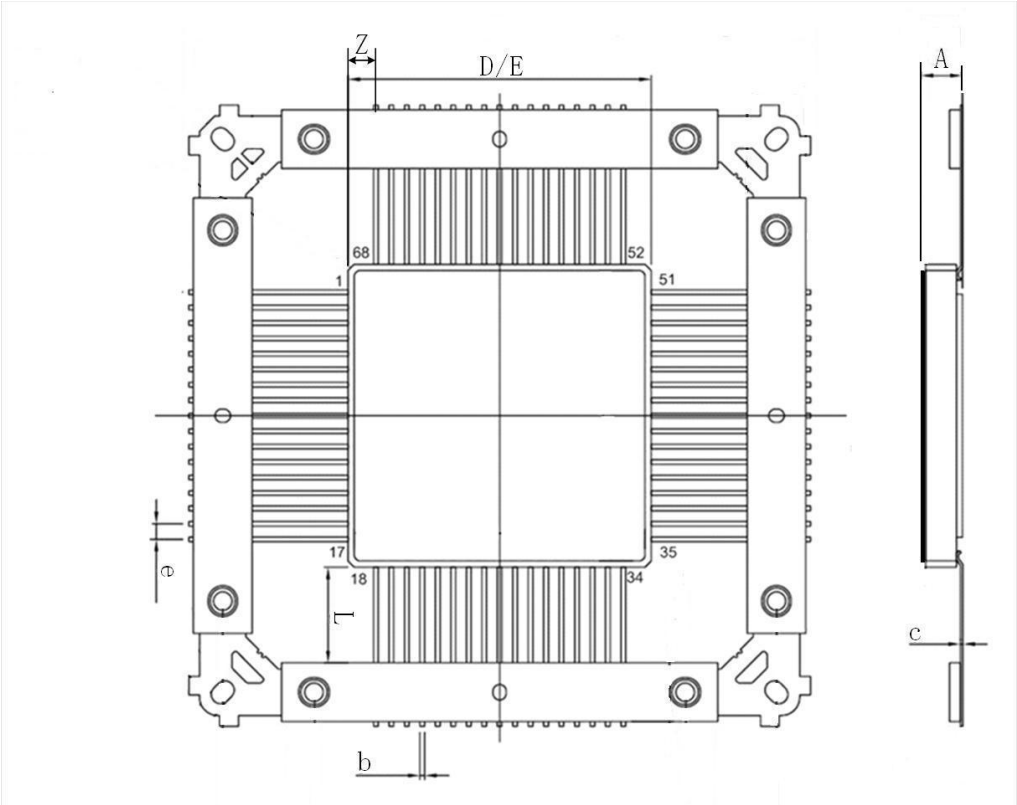
Symbol	Parameter	Limits		Unit
		Minimum	maximum	
V_{DD}	Supply voltage	-0.5	7.0	V
V_I	DC input voltage	-0.5	V_{DD}+0.5	V
V_O	DC output voltage	-0.5	V_{DD}+0.5	V
T_{STG}	Storage Temperature	-65	150	℃
P_D	Maximum power dissipation	—	3.5	W
T_J	Maximum junction temperature	—	+150	℃
I_I	DC input current	-10	10	mA
$R_{th(J-C)}$	Thermal resistance, junction-to-case	—	28	℃/W

8. Typical Application（Appendix 2）

9. Packaging

The SRAM B65608EARH utilizes 68-Lead Ceramic Quad Flatpack as in Figure

11 and the corresponding dimensions are listed in Table 10.



Notes:

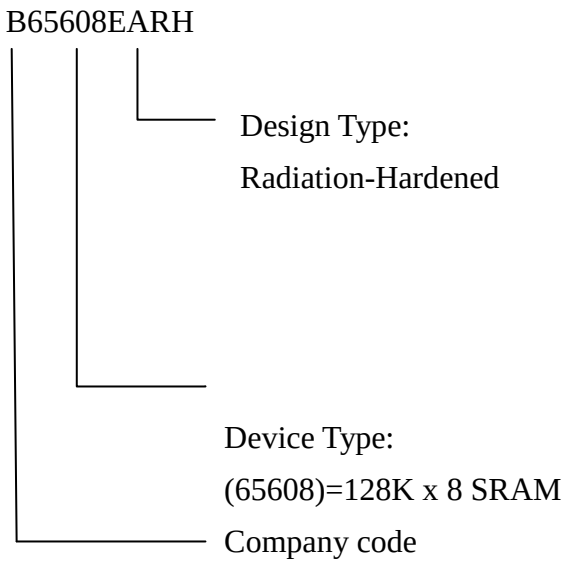
1. The lid is electrically connected to VSS.

Figure 11. Package Outline

Table 10. Package Dimensions

Symbol	Value (Unit: mm)		
	Min	Normal	Max
A	3.0	--	3.7
b	0.31	--	0.45
c	0.14	--	0.26
e	--	1.27	--
D/E	24.5	--	25.3
L	7.5	--	8.3
Z	--	--	2.54

10. Naming Rule



Appendix 1

Pin Descriptions are listed in Table 11：

Table 11. Pin Symbols and Functions (Ⅰ)

Pin NO.	Symbol	Functions	Pin NO.	Symbol	Functions
1	NC	No Connect	35	NC	No Connect
2	NC	No Connect	36	NC	No Connect
3	NC	No Connect	37	NC	No Connect
4	DQ0	I/O	38	NC	No Connect
5	DQ1	I/O	39	DQ4	I/O
6	NC	No Connect	40	DQ5	I/O
7	NC	No Connect	41	NC	No Connect
8	NC	No Connect	42	NC	No Connect
9	V_{SS}	Ground	43	V_{SS}	Ground
10	NC	No Connect	44	NC	No Connect
11	NC	No Connect	45	NC	No Connect
12	DQ2	I/O	46	NC	No Connect
13	DQ3	I/O	47	DQ6	I/O
14	NC	No Connect	48	DQ7	I/O
15	NC	No Connect	49	NC	No Connect
16	NC	No Connect	50	NC	No Connect
17	NC	No Connect	51	NC	No Connect
18	V_{DD}	Power	52	V_{DD}	Power
19	A11	Address	53	A10	Address
20	A12	Address	54	A9	Address
21	A13	Address	55	A8	Address
22	A14	Address	56	A7	Address
23	A15	Address	57	A6	Address

24	A16	Address	58	$\overline{W}$	Write Enable
25	$\overline{E1}$	Chip Enable 1	59	NC	No Connect
26	$\overline{G}$	Output Enable	60	V_{SS}	Ground
27	E2	Chip Enable 2	61	NC	No Connect

Table 11. Pin Symbols and Functions (Ⅱ)

Pin NO.	**Symbol**	**Functions**	**Pin NO.**	**Symbol**	**Functions**
28	V_{DD}	Power	62	A5	Address
29	V_{SS}	Ground	63	A4	Address
30	NC	No Connect	64	A3	Address
31	NC	No Connect	65	A2	Address
32	NC	No Connect	66	A1	Address
33	V_{DD}	Power	67	A0	Address
34	V_{SS}	Ground	68	V_{SS}	Ground

Appendix 2

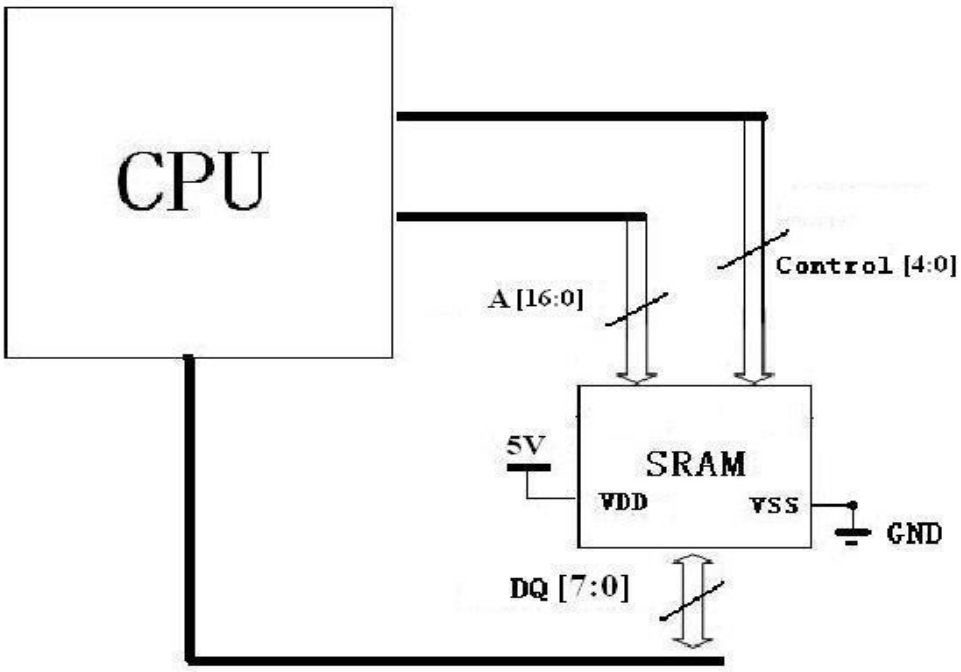


Figure 12. Typical Application

Figure 11 illustrates a typical application system, which consists of a CPU and an SRAM (B65608EARH) chip. The B65608EARH serves as data storage for the CPU, while the CPU controls the SRAM operation properly.

For starting up normally, 5V power supply should be applied to the SRAM correctly; thereafter it will operate according to the control signals sent by the CPU. Normally the CPU will write some data into the SRAM in the first place. For this operation, $\overline{W}$ should be set lower than V_{IH}, and either of two different write cycles described in Section 7.3 can be used to realize the writing, as long as the signals generated by the CPU satisfy the relevant timing sequence requirements.

The read operation can be implemented similarly, except that $\overline{W}$ should be deasserted primarily. The B65608EARH offers three different kinds of read cycles, the selection of which can be decided according to the demand of whole system. Also, proper signal sequence is required for successful read operation.

Service & Supply

Address: No.2. Siyingmen N.Rd. Donggaodi Fengtai District,BeiJing,China
Department: Department of international cooperation
Telephone: +86(0)10-67968115-6751
Email：gjhz@mxtronics.com
Fax: +86(0)10-68757706
Zip code: 100076