Ver 1.2

Radiation-Hardened SRAM

Datasheet

Part Number：B8CR256K32RH

中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

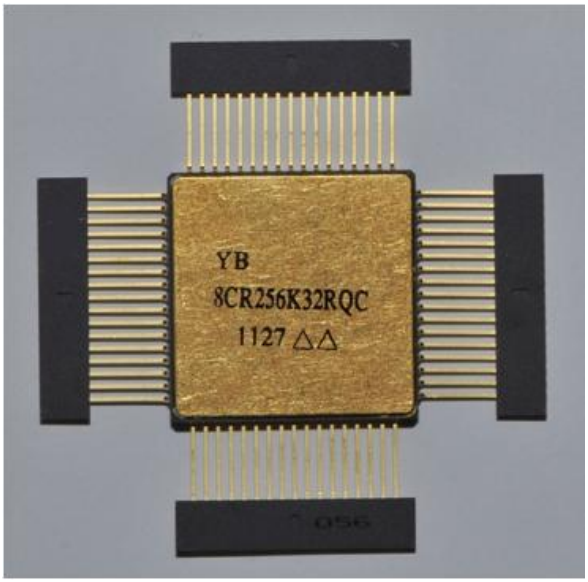
Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	09.20.2016		Document creation	
1.1	03.26.2017		ADVANCE INFORMATION DATASHEET Document	
1.2	03.06.2018		Text and wording modifications	

TABLE OF CONTENTS

1. Features 1
2. General Description 1
3. Block Diagram 2
4. Pin Description 2
5. Pin Configurations（Appendix 1） 3
6. Product Description 3
6.1 Quality Grade and Production Standard 3
6.2 Function Description 3
6.3 AC Test Load and Input Waveforms 7
6.4 Recommended Operating Conditions 7
7. Electrical Characteristics 7
7.1 DC Electrical Characteristics (Pre and Post-Radiation) 7
7.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation) 10
7.3 Write Cycle AC Electrical Characteristics (Pre and Post-Radiation) 13
7.4 Absolute Maximum Ratings 16
8. Typical Application（Appendix 2） 16
9. Packaging 16
10. Naming Rule 18
Appendix 1 19
Appendix 2 21

1. Features

- 25 ns maximum access time
- Asynchronous operation
- CMOS compatible inputs and output levels, three-state bidirectional data bus
- I/O Voltage 3.3 V，1.8 V core
- ESD better than 2000 V
- Operational environment:
  Total-dose: 100 K Rad (Si)
  SEL Immune: > 75 MeV cm^2/mg
  SEU Error Rate=1E-10errors/bit-day in Geosynchronous Orbit
- Packaging options
  68-lead ceramic quad flatpack（QFP68）



2. General Description

The B8CR256K32RH is a high-performance radiation-hardened CMOS static RAM organized as 262,144 words by 32 bits. Fabricated with industry-standard CMOS technology, the device works in asynchronous mode and requires no external clocks. The combination of radiation-hardness, fast access time, and low power consumption makes the B8CR256K32RH ideal for high speed system designed for operation in radiation environments.

3. Block Diagram

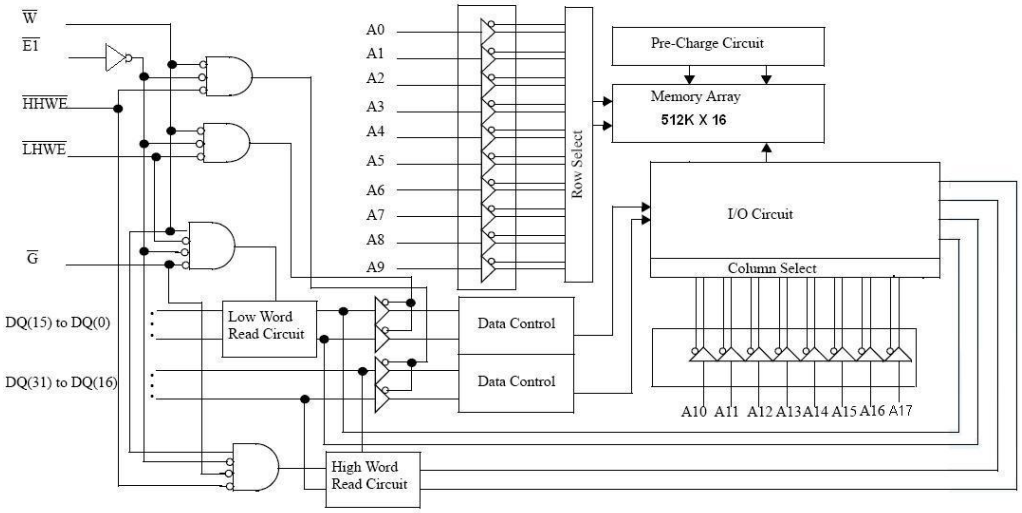


Figure 1. B8CR256K32RH Block Diagram

4. Pin Description

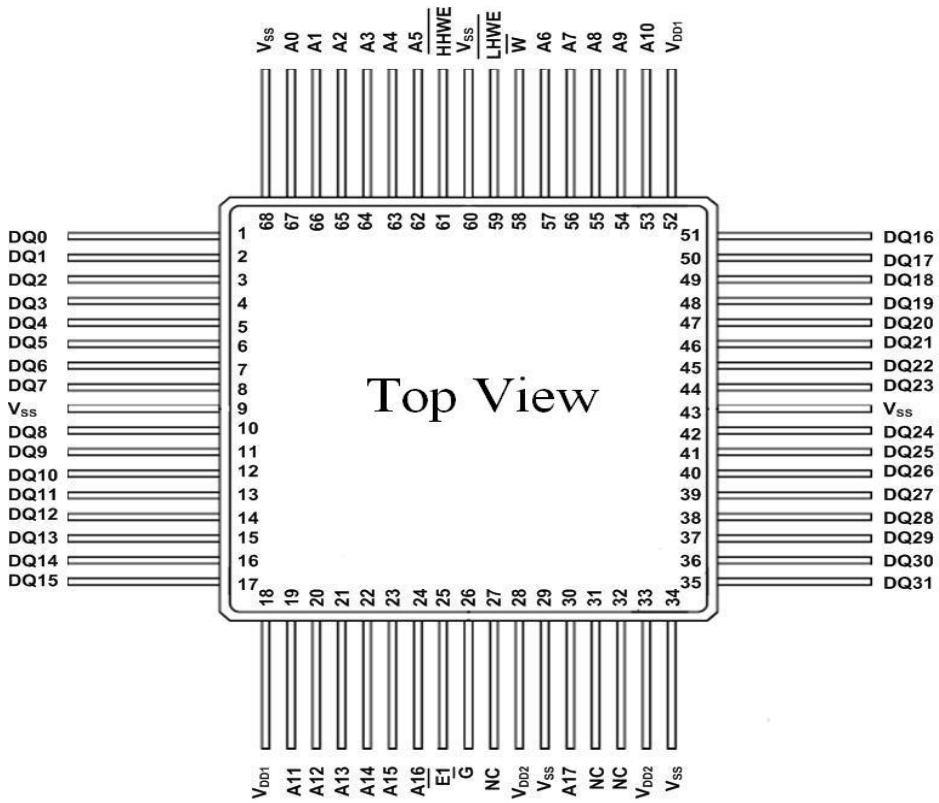


Figure 2. B8CR256K32RH SRAM Pinout (68)

Table 1. Pin Names

Pin Names	Functions
A0~A17	Address
D0~D31	Data Input / Output
$\overline{E1}$	Chip Enable 1 (Active Low)
$\overline{W}$	Write Enable (Low Write Enable, and High Read Enable)
$\overline{G}$	Output Enable (Active Low)
$\overline{LHWE}$	Low half-word enable
$\overline{HHWE}$	High half-word enable
VDD1	Power (1.8 V)
VDD2	Power (3.3 V)
VSS	Ground
NC	No Connect

5. Pin Configurations（Appendix 1）

6. Product Description

6.1 Quality Grade and Production Standard

The quality grade of the radiation-hardened SRAM B8CR256K32RH is GJB597A-1996 B. And B8CR256K32RH is up to the HQZX4-2011 semiconductor IC standard and CASTPSW11/338-2011 standard.

6.2 Function Description

The B8CR256K32RH has five control inputs called Chip Enable 1 ($\overline{E1}$), Write

Enable ($\overline{W}$), Half-word Enables ($\overline{HHWE}$/$\overline{LHWE}$) and Output Enable ($\overline{G}$); 18 address inputs, A (17:0); and 32 bidirectional data lines, DQ (31:0).

Table 2. Device Operation Truth Table

Inputs					Outputs	
$\overline{G}$	$\overline{W}$	$\overline{E1}$	$\overline{LHWE}$	$\overline{HHWE}$	I/O Mode	Mode
X	X	1	X	X	DQ(31:16) 3-State DQ(15:0) 3-State	Standby
X	X	X	X	X	DQ(31:16) 3-State DQ(15:0) 3-State	Standby
0	1	0	0	1	DQ(31:16) 3-State DQ(15:0) Data out	Low Half-Word Read
0	1	0	1	0	DQ(31:16) Data out DQ(15:0) 3-state	High Half-Word Read
0	1	0	0	0	DQ(31:16) Data out DQ(15:0) Data out	Word Read
X	0	0	0	0	DQ(31:16) Data in DQ(15:0) Data in	Word Write
X	0	0	0	1	DQ(31:16) 3-State DQ(15:0) Data in	Low Half-Word Write
X	0	0	1	0	DQ(31:16) Data in DQ(15:0) 3-State	High Half-Word Write
1	1	0	X	X	DQ(31:16) 3-State DQ(15:0) 3-State	3-State
X	X	0	1	1	DQ(31:16) 3-State DQ(15:0) 3-State	3-State

Notes:

1. X = Don’t care

◆ **Read Cycle**

A combination of $\overline{W}$ greater than V_{IH}(min) and $\overline{E1}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 4, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ (31:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enables and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5, is initiated by $\overline{E1}$ going active while $\overline{G}$ remains asserted，$\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 32-bit word addressed by A (17:0) is accessed and appears at the data outputs DQ (31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 6, is initiated by $\overline{G}$ going active while $\overline{E1}$ are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

◆ **Write Cycle**

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 7, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 32 bidirectional pins DQ (31:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 8, is defined by a write terminated by $\overline{E1}$ going inactive. The write pulse width is defined by t_{WLEF}

when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by $\overline{E1}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the 32 bidirectional pins DQ (31:0) to avoid bus contention.

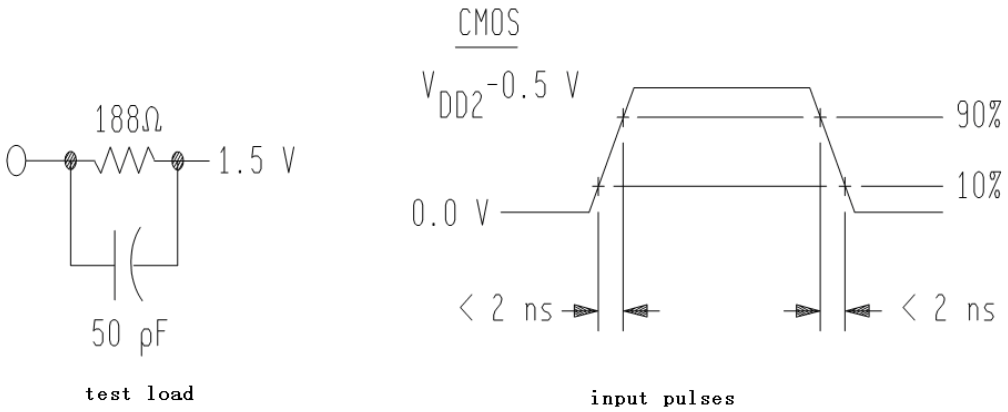
◆ **Word Enables**

Separate half-word enable controls ($\overline{HHWE}$ and $\overline{LHWE}$) allow individual 16-bit word accesses. $\overline{LHWE}$ controls the lower bits DQ (15:0). $\overline{HHWE}$ controls the upper bits DQ (31:16). Writing to the device is performed by asserting $\overline{E1}$ and the half-word enables. Reading the device is performed by asserting $\overline{E1}$, $\overline{G}$ and the half-word enables while $\overline{W}$ is held inactive (HIGH).

Table 3. Separate half-word enable operation

$\overline{HHWE}$	$\overline{LHWE}$	operation
0	0	32-bit read or write cycle
0	1	16-bit high half-word read or write cycle (low half-word bi-direction pins DQ(15:0) are in 3-state)
1	0	16-bit low half-word read or write cycle (high half-word bi-direction pins DQ(31:16) are in 3-state)
1	1	High and low half-word bi-directional pins remain in 3-state, write function disabled

6.3 AC Test Load and Input Waveforms



Notes: 1. 50pF includes scope probe and test socket capacitance.

2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = V_{DD2}/ 2)

Figure.3 AC Test Load and Input Waveforms

6.4 Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	1.7 V ~ 1.9 V
V_{DD2}	I/O supply voltage	3.0 V ~ 3.6 V
T_C	Case temperature range	-55℃ ~ +125℃
V_I	DC input voltage	0 V ~ V_{DD2}

Notes:

The correct power-up sequence should be V_{DD1}--> V_{DD2}.

7. Electrical Characteristics

7.1 DC Electrical Characteristics (Pre and Post-Radiation)

Table 5. DC Parameter Table (Ⅰ)

Parameter	Symbol	Condition （GND=0V，-55℃≤T_A≤125℃ ） 1.7V≤V_{DD1}≤1.9V、3.0V≤V_{DD2}≤3.6V	Limits		UNIT
			MIN	MAX	
High-level input voltage	V_{IH}		.7*V_{DD2}	—	V
Low-level input voltage	V_{IL}		—	.3*V_{DD2}	V
High-level output voltage	V_{OH}	V_{DD2}=3V, I_{OH}=-4 mA, all outputs needed are tested	.8*V_{DD2}	—	V
Low-level output voltage	V_{OL}	V_{DD2}=3V, I_{OL}=8 mA, all outputs needed are tested	—	.2*V_{DD2}	V
Input capacitance	C_{IN}[1]	f=1MHz@0V		24	pF
Bidirectional I/O Capacitance	C_{IO}[1]	f=1MHz@0V		24	pF
High-level input leakage current	I_{IH}	V_{DD2}=3.6V, V_{DD1}=1.9V, V_I=3.6V, all inputs are tested	-4	4	μA
Low-level input leakage current	$\|I_{IL}\|$	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_I= 0V, all inputs are tested	-4	4	μA
Three-state (high-level) output leakage current	I_{OZH}	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_O=V_{DD2}, all bidirectional I/O are tested	-4	4	μA
Three-state (low-level) output leakage current	$\|I_{OZL}\|$	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_O=0, all bidirectional I/O are tested	-4	4	μA
Core Supply current operating @1MHz	$I_{DD1}(OP_1)$	V_{IL}=0.2V, V_{IH} =3.4V, I_{DD1} current is tested V_{DD1}=1.9V		65	mA
Core Supply current operating @40MHz	$I_{DD1}(OP_2)$	V_{IL}=0.2V, V_{IH} =3.4V, I_{DD1} current is tested V_{DD1}=1.9V		150	mA mA

I/O Supply current operating @1 MHz	$I_{DD2}(OP_1)$	V_{IL}=0.2V, V_{IH}=3.4V, V_{DD1}=1.9V, V_{DD2}=3.6V, I_{DD2} current is tested		2	mA
I/O Supply current operating @40 MHz	$I_{DD2}(OP_2)$	V_{IL}=0.2V, V_{IH}=3.4V, V_{DD1}=1.9V, V_{DD2}=3.6V, I_{DD2} current is tested		24	mA

Table 5. DC Parameter Table (Ⅱ)

Parameter	Symbol	Condition （GND=0V，-55℃≤T_A≤125℃ ） 1.7V≤V_{DD1}≤1.9V、3.0V≤V_{DD2}≤3.6V	Limits		UNIT
			MIN	MAX	
Supply current standby @0 Hz	$I_{DD1}(SB)$	CMOS inputs,I_{OUT}=0，$\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		60	mA
Supply current standby @0 Hz	$I_{DD2}(SB)$	CMOS inputs,I_{OUT}=0，$\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}=3.6V, V_{DD1}=1.9V		400	μA
Supply current standby A (16:0) @40M Hz	$I_{DD1}(SB)$	CMOS inputs,I_{OUT}=0，$\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		60	mA
Supply current standby A (16:0) @40M Hz	$I_{DD2}(SB)$	CMOS inputs,I_{OUT}=0，$\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		400	μA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.

3. Not more than one output may be shorted at a time for maximum duration of one second.
4. $V_{IH}=V_{DD2}$.

7.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 6. Read Cycle AC Parameters (Ⅰ)

Parameter	Symbol	Condition ($V_{DD1}=V_{DD1}$(min), $V_{DD2}=V_{DD2}$(min), -55 ℃ ≤ T_A ≤ 125 ℃)	Limits		UNIT
			MIN	MAX	
Read cycle time	t_{AVAV}[1]	Figure 4	25	—	ns
Address to data valid	t_{AVQV}		—	25	ns
Output hold time from address change	t_{AXQX}[2]		3	—	ns
$\overline{G}$-controlled output enable time	t_{GLQX}[2,1]	Figure 6	0	—	ns
$\overline{G}$-controlled output data valid	t_{GLQV}		—	10	ns
$\overline{G}$-controlled output three-state time	t_{GHQZ}[2]		—	7	ns
$\overline{E}$ 1-controlled output enable time	t_{ETQX}[2,3]	Figure 5	3	—	ns
$\overline{E}$ 1-controlled access time	t_{ETQV}[3]		—	25	ns

$\overline{E1}$-controlled output three-state time	t_{EFQZ}[2,4]		—	10	ns
$\overline{HHWE}$, $\overline{LHWE}$ enable to output in Low-z	t_{BLQX}[1]	Figure 6	0	—	ns

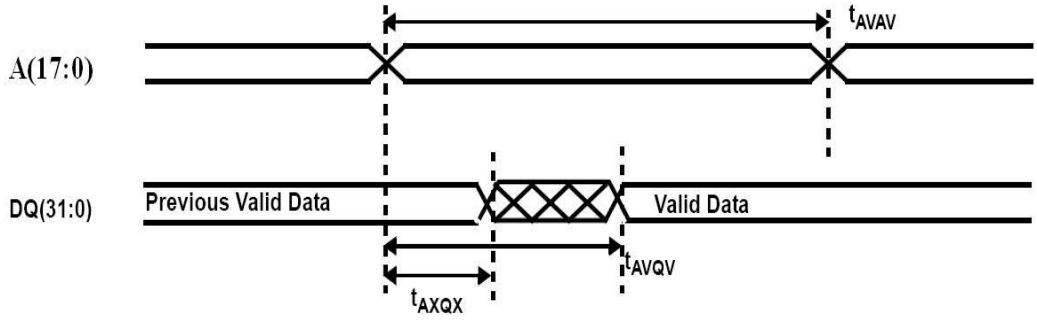
Table 6. Read Cycle AC Parameters (Ⅱ)

Parameter	Symbol	Condition (V_{DD1}=V_{DD1}(min), V_{DD2}=V_{DD2}(min), -55 ℃ ≤ T_A≤ 125 ℃)	Limits		UNIT
			MIN	MAX	
$\overline{HHWE}$, $\overline{LHWE}$ enable to output in High-z	t_{BHQZ}		—	10	ns
$\overline{HHWE}$, $\overline{LHWE}$ enable to data valid	t_{BLQV}		—	10	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

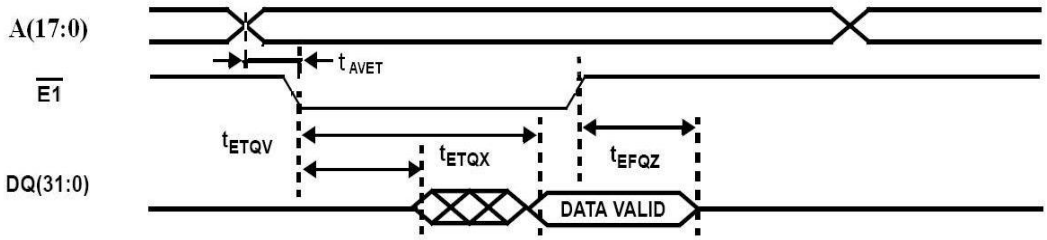
1. Guaranteed but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (chip enable true) notation refers to the falling edge of $\overline{E1}$.
4. The EF (chip enable false) notation refers to the rising edge of $\overline{E1}$.



Assumptions:

$\overline{E1}$ ≤V_{IL}(max), $\overline{G}$≤V_{IL}(max), $\overline{W}$≥V_{IH}(min)

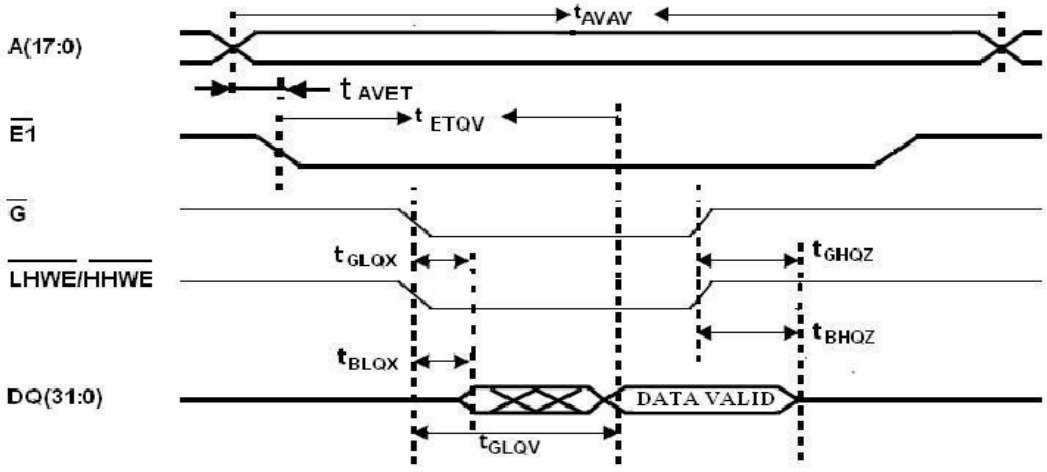
Figure 4. SRAM Read Cycle 1: Address Access



Assumptions：

1. $\overline{G}$, $\overline{HHWE}$, $\overline{LHWE}$≤V_{IL}(max), $\overline{W}$≥V_{IH}(min)
2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 5. SRAM Read Cycle 2: Chip Enable Access



Assumptions:

1. $\overline{W} \geq V_{IH}(min)$
2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 6. SRAM Read Cycle 3: Output Enable Access

7.3 Write Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 7. Write Cycle AC Parameter (Ⅰ)

Parameter	Symbol	Condition ($V_{DD1}=V_{DD1}(min)$, $V_{DD2}=V_{DD2}(min)$, $-55℃ \leq T_A \leq 125℃$)	Limits		UNIT
			MIN	MAX	
Write cycle time	t_{AVAV}[1]	Figure 7 & Figure 8	25		ns
Chip enable to end of write	t_{ETWH}	Figure 7	20	—	ns
Address setup time for write ($\overline{E}$1 /E2-controlled)	t_{AVET}		2	—	ns

Table 7. Write Cycle AC Parameter (Ⅱ)

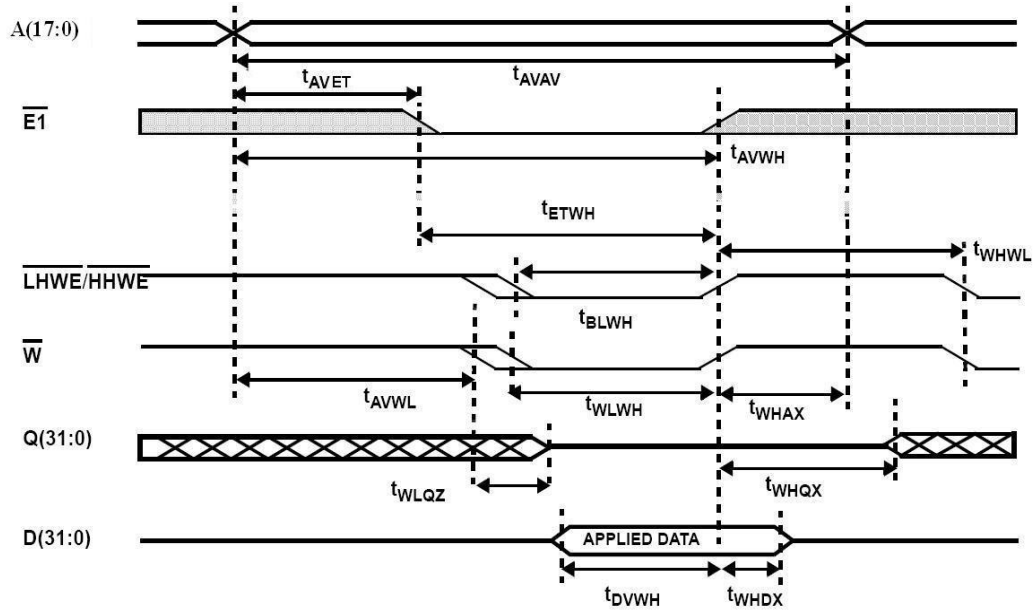
parameter	symbol	Condition ($V_{DD1}=V_{DD1}(min)$, $V_{DD2}=V_{DD2}(min)$, $-55℃ \leq T_A \leq 125℃$)	Limits		UNIT
			MIN	MAX	
Address setup time for write ($\overline{W}$ -controlled)	t_{AVWL}	Figure 7	2	—	ns
Write pulse width	t_{WLWH}	Figure 7	20	—	ns
Address hold time for write ($\overline{W}$ -controlled)	t_{WHAX}	Figure 7	3	—	ns

Address hold time for chip enable ($\overline{E1}$/E2-controlled)	t_{EFAX}	Figure 8	3	—	ns
$\overline{W}$-controlled three-state time	t_{WLQZ}[2]	Figure 7	—	10	ns
$\overline{W}$-controlled output enable time	t_{WHQX}[2]	Figure 7	5	—	ns
Chip enable pulse width ($\overline{E1}$/E2-controlled)	t_{ETEF}	Figure 8	20	—	ns
Data setup time	t_{DVWH}	Figure 7	15	—	ns
Data hold time	t_{WHDX}	Figure 7	5	—	ns
Chip enable controlled write pulse width	t_{WLEF}	Figure 8	20	—	ns
Data setup time	t_{DVEF}	Figure 8	15	—	ns
Data hold time	t_{EFDX}	Figure 8	5	—	ns
Address valid to end of write	t_{AVWH}	Figure 7	20	—	ns
Write disable time	t_{WHWL}[1]	Figure 7	5	—	ns
$\overline{HHWE}$, $\overline{LHWE}$ low to write high	t_{BLWH}	Figure 7	20	—	ns
$\overline{HHWE}$, $\overline{LHWE}$ low to enable high	t_{BLEF}	Figure 8	20	—	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

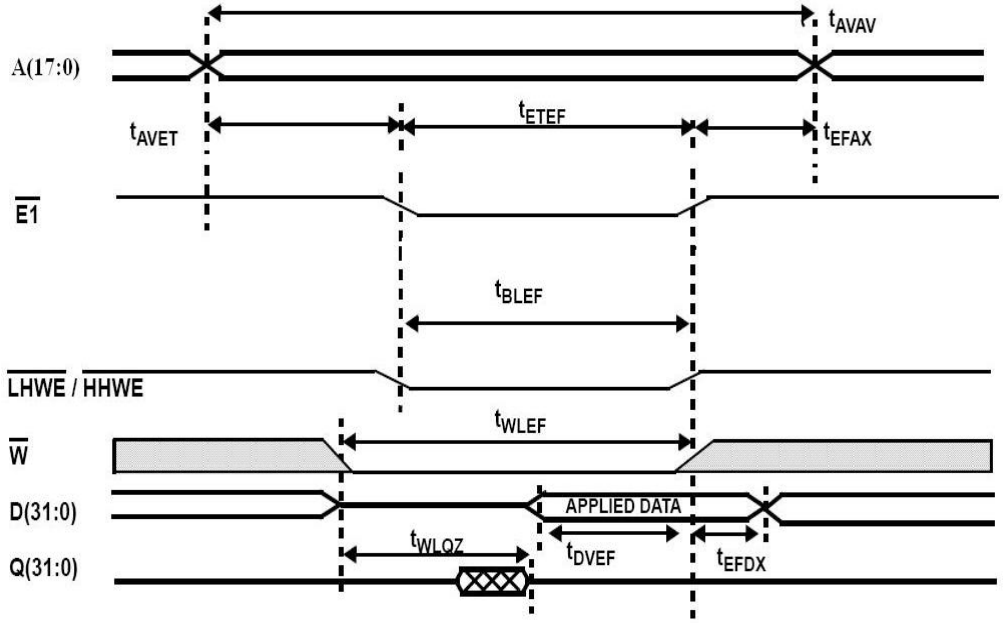
1. Tested with $\overline{G}$ high.
2. Three-state is defined as 200mV change from steady-state output voltage.



Assumption:

1. $\overline{G} \leq V_{IL}(max)$
2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 7. SRAM Write Cycle 1: $\overline{W}$-controlled Access



Assumption:

1. $\overline{G} \leq V_{IL}(max)$

2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 8. SRAM Write Cycle 2: Enable-chip Controlled Access

7.4 Absolute Maximum Ratings

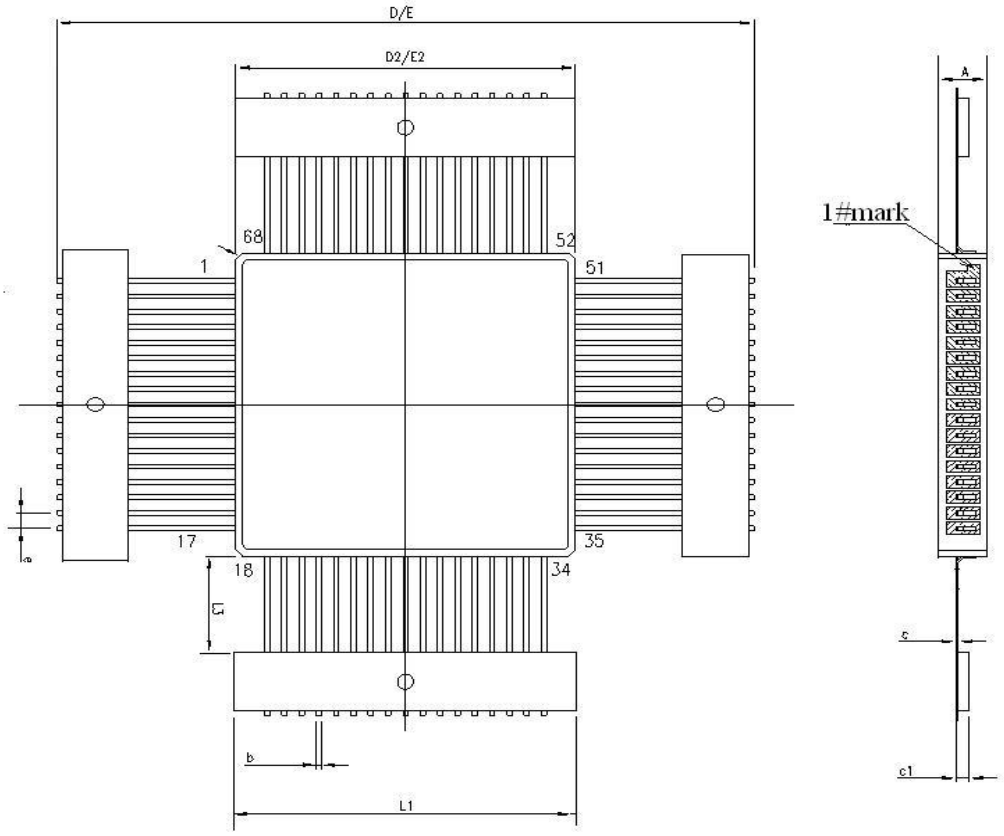
Table 8. Absolute Maximum Ratings

Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	-0.3V ~ +2.1 V
V_{DD2}	I/O supply voltage	-0.3V ~ +3.8 V
$V_{I/O}$	Voltage on any pin	-0.3V ~ +3.8 V
T_{STG}	Storage Temperature	-65℃ ~ 150℃
P_D	Maximum power dissipation	2.4W
T_J	Maximum junction temperature	+175℃
I_I	DC input current	±5 mA
$R_{th(J-C)}$	Thermal resistance, junction-to-case	5℃/W

8. Typical Application（Appendix 2）

9. Packaging

The SRAM B8CR256K32RH utilizes 68-Lead Ceramic Quad Flatpack, as in Figure 9 and the corresponding dimensions are listed in Table 9.



Notes:

1. The lid is electrically connected to VSS.

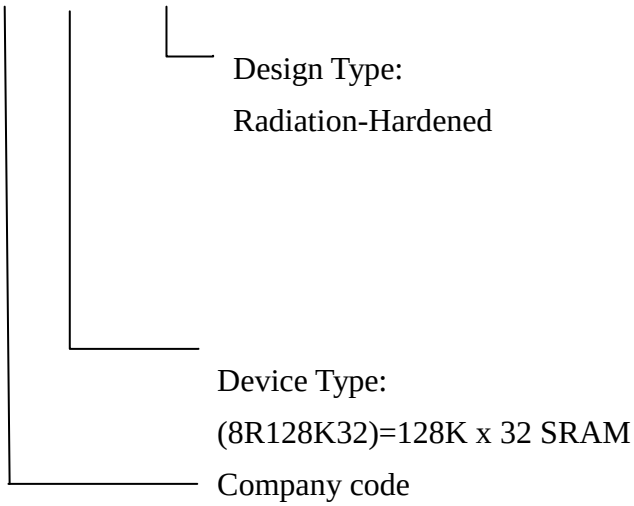
Figure 9. Package Outline

Table 9. Package Dimensions

Symbol	Value (Unit: mm)		
	Min	Normal	Max
A	3.60	--	4.30
b	0.33	--	0.43
c	0.15	--	0.25
c1	7.6	8.9	10.2
e	--	1.27	--
D/E	--	52.39	--
D2/E2	24.64	--	25.14
L1	23.89	--	24.37
L3	--	7.87	--

10. Naming Rule

B8CR256K32RH



Appendix 1

Pin Descriptions are listed in Table 10：

Table 10. Pin Symbols and Functions (Ⅰ)

Pin NO.	Symbol	Functions	Pin NO.	Symbol	Functions
1	DQ0	I/O	35	DQ31	I/O
2	DQ1	I/O	36	DQ30	I/O
3	DQ2	I/O	37	DQ29	I/O
4	DQ3	I/O	38	DQ28	I/O
5	DQ4	I/O	39	DQ27	I/O
6	DQ5	I/O	40	DQ26	I/O
7	DQ6	I/O	41	DQ25	I/O
8	DQ7	I/O	42	DQ24	I/O
9	V_{SS}	Ground	43	V_{SS}	Ground
10	DQ8	I/O	44	DQ23	I/O
11	DQ9	I/O	45	DQ22	I/O
12	DQ1O	I/O	46	DQ21	I/O
13	DQ11	I/O	47	DQ20	I/O
14	DQ12	I/O	48	DQ19	I/O
15	DQ13	I/O	49	DQ18	I/O
16	DQ14	I/O	50	DQ17	I/O
17	DQ15	I/O	51	DQ16	I/O
18	V_{DD1}	Power (1.8V)	52	V_{DD1}	Power (1.8V)
19	A11	Address	53	A10	Address
20	A12	Address	54	A9	Address
21	A13	Address	55	A8	Address
22	A14	Address	56	A7	Address
23	A15	Address	57	A6	Address
24	A16	Address	58	$\overline{W}$	Write Enable

Table 10. Pin Symbols and Functions (Ⅱ)

Pin NO.	Symbol	Functions	Pin NO.	Symbol	Functions
25	$\overline{E1}$	Chip Enable 1	59	$\overline{LHWE}$	Low half-word enable
26	$\overline{G}$	Output Enable	60	V_{SS}	Ground
27	NC	No connect	61	$\overline{HHWE}$	High half-word enable
28	V_{DD2}	Power (3.3V)	62	A5	Address
29	V_{SS}	Ground	63	A4	Address
30	A17	Address	64	A3	Address
31	NC	No Connect	65	A2	Address
32	NC	No Connect	66	A1	Address
33	V_{DD2}	Power (3.3V)	67	A0	Address
34	V_{SS}	Ground	68	V_{SS}	Ground

Appendix 2

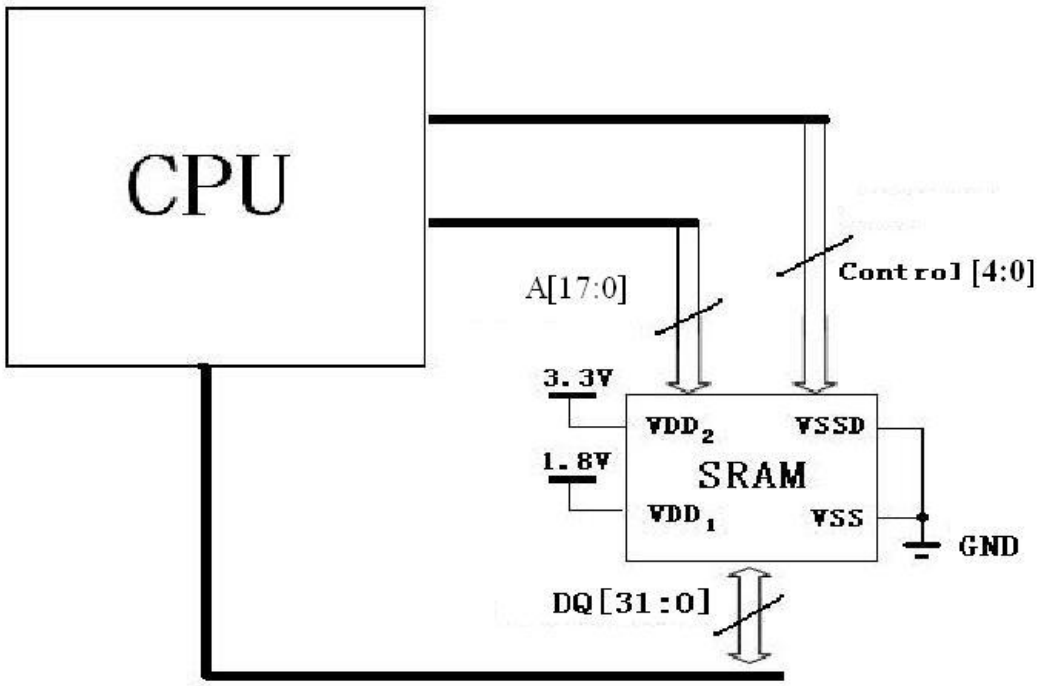


Figure 10. Typical Application

Figure 10 illustrates a typical application system, which consists of a CPU and an SRAM (B8CR256K32RH) chip. The B8CR256K32RH serves as data storage for the CPU, while the CPU controls the SRAM operation properly.

For starting up normally, both 3.3 and 1.8 V power supply should be applied to the SRAM correctly, and then it will operate according to the control signals sent by the CPU. Normally the CPU will write some data into the SRAM in the first place. For this operation, $\overline{W}$ should be set lower than V_{IH}, and either of two different write cycles described in Section 7.3 can be used to realize the writing, as long as the signals generated by the CPU satisfy the relevant timing sequence requirements.

The read operation can be implemented similarly, except that $\overline{W}$ should be deasserted primarily. The B8CR256K32RH offers three different kinds of read cycles, the selection of which can be decided according to the demand of whole system. Also, proper signal sequence is required for successful read operation.

Service & Supply

Address: No.2. Siyingmen N.Rd. Donggaodi Fengtai District,BeiJing,China

Department: Department of international cooperation

Telephone: +86(0)10-67968115-6751

Email：gjhz@mxtronics.com

Fax: +86(0)10-68757706

Zip code: 100076