Ver 1.1

16-Bit 400MSPS Digital to Analog Converter

Datasheet

Part Number：B9726RHQN

中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

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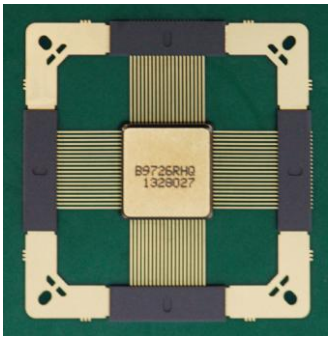
1. Unique Features



- High speed LVDS interface
- LVDS inputs with internal 150 Ω terminations
- Single data rate or double data rate capable
- Default data input: twos complement binary format
- Internal precision reference
- Operates on 2.5 V and 3.3 V supplies
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV ·cm^2/mg

2. Product Description

The B9726RHQN is a radiation hardened ,16-bit digital-to-analog converter (DAC) that offers leading edge performance at conversion rates of up to 400 MSPS. The device uses low voltage differential signaling (LVDS) inputs and includes internal 150Ω terminations. The analog output can be single-ended or differential current. An internal precision reference is included.

The B9726RHQN also features synchronization logic to monitor and optimize the timing between incoming data and the sample clock. This reduces system complexity and simplifies timing requirements. An LVDS clock output is also available to drive an external data pump in either single data rate (SDR) or double data rate (DDR) mode.

All device operation is fully programmable using the flexible serial port interface (SPI). The B9726RHQN is also fully functional in its default state for applications without a controller.

3. Functional Block Diagram

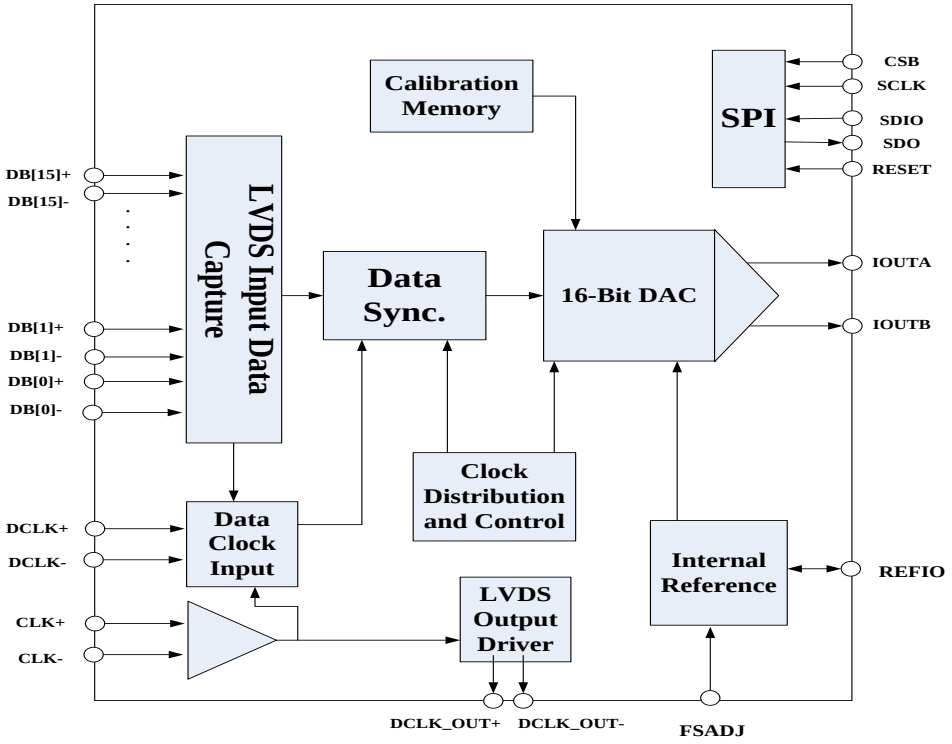


Figure 3-1. Block Diagram

4. Pin Description

The B9726RHQN is packaged in CQFP80 package, as is shown in figure 4-1.

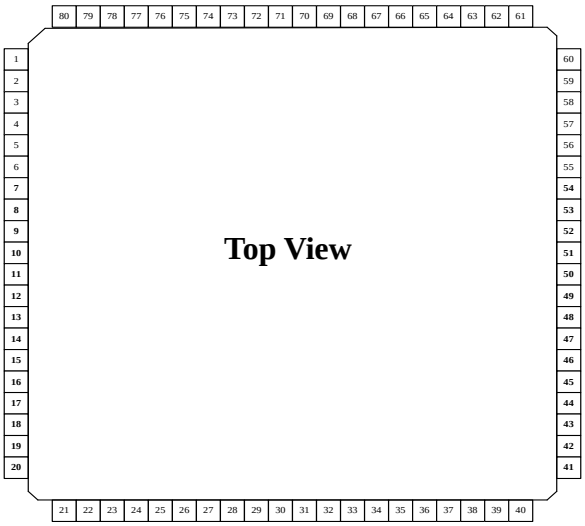


Figure 4-1. B9726RHQN Top View

Table 4-1. Pin Description

Symbol	Description
DB0+~15+	Data Input Bit True（LSB~MSB）
DB0-~15-	Data Input Bit Complement（LSB~MSB）
REXT	Sets Data Clock Output Driver
CLK+、CLK-	DAC Clock Input
DCLK_OUT+、DCLK_OUT-	Data Clock Output
DCLK+、DCLK-	Data Clock Input
SDO	SPI Data Output
SDIO	SPI Data Input/Output
SCLK	SPI Clock Input
CSB	SPI Chip Select Bar(Active Low)
RESET	Hardware Reset(Active High)
REFIO	Internal Reference Input/Output
FSADJ	Output Current Full-Scale Adjust
SDR_EN	Single Data Rate Mode Enable
IOUTB	Analog Current Output Complement
IOUTA	Analog Current Output True
SPI_DIS	Serial Port Interface Disable
EPAD	Analog Ground. Should be connected to ground for electrical and thermal purposes
V_{DD2}	2.5V Power Supply
V_{DD1}	3.3V Power Supply
GND	Ground

5. Pin Definition

Table 5-1. Pin definition

Pin NO.	Symbol	Description	Pin NO.	Symbol	Description
1	V_{DD2}	2.5V Power Supply	41	GND	Ground
2	REXT [1]	Sets Data Clock Output Driver	42	DB4+	Data Input Bit 4 True
3	V_{DD2}	2.5V Power Supply	43	DB4-	Data Input Bit 4 Complement
4	GND	Ground	44	DB3+	Data Input Bit 3 True
5	CLK+	DAC Clock Input True	45	DB3-	Data Input Bit 3 Complement
6	CLK-	DAC Clock Input Complement	46	DB2+	Data Input Bit 2 True
7	GND	Ground	47	DB2-	Data Input Bit 2 Complement
8	GND	Ground	48	DB1+	Data Input Bit 1 True
9	V_{DD2}	2.5V Power Supply	49	DB1-	Data Input Bit 1 Complement
10	DB15+	Data Input Bit 15 True(MSB)	50	DB0+	Data Input Bit 0 True
11	DB15-	Data Input Bit 15 Complement	51	DB0-	Data Input Bit 0 Complement

Pin NO.	Symbol	Description	Pin NO.	Symbol	Description
12	DB14+	Data Input Bit 14 True	52	V_{DD2}	2.5V Power Supply
13	DB14-	Data Input Bit 14 Complement	53	GND	Ground
14	DB13+	Data Input Bit 13 True	54	SDO	SPI Data Input
15	DB13-	Data Input Bit 13 Complement	55	SDIO	SPI Data Input/Output
16	DB12+	Data Input Bit 12 True	56	SCLK	SPI Clock Input
17	DB12-	Data Input Bit 12 Complement	57	CSB	SPI Chip Select Bar(Active Low)
18	DB11+	Data Input Bit 11 True	58	RESET	Hardware Reset(Active High)
19	DB11-	Data Input Bit 11 Complement	59	REFIO [2]	Internal Reference Input/Output
20	V_{DD1}	3.3V Power Supply	60	FSADJ [3]	Output Current Full-Scale Adjust
21	GND	Ground	61	SDR_EN [4]	Single Data Rate Mode Enable
22	DB10+	Data Input Bit 10 True	62	V_{DD2}	2.5V Power Supply
23	DB10-	Data Input Bit 10 Complement	63	GND	Ground
24	DB9+	Data Input Bit 9 True	64	V_{DD2}	2.5V Power Supply
25	DB9-	Data Input Bit 9 Complement	65	GND	Ground
26	DB8+	Data Input Bit 8 True	66	V_{DD1}	3.3V Power Supply
27	DB8-	Data Input Bit 8 Complement	67	GND	Ground
28	DCLK_OUT+	Data Clock Output True	68	V_{DD1}	3.3V Power Supply
29	DCLK_OUT-	Data Clock Output Complement	69	GND	Ground
30	V_{DD1}	3.3V Power Supply	70	IOUTB	Analog Current Output Complement
31	GND	Ground	71	IOUTA	Analog Current Output True
32	DCLK+	Data Clock Input True	72	GND	Ground
33	DCLK-	Data Clock Input Complement	73	V_{DD1}	3.3V Power Supply
34	DB7+	Data Input Bit 7 True	74	GND	Ground
35	DB7-	Data Input Bit 7 Complement	75	V_{DD1}	3.3V Power Supply
36	DB6+	Data Input Bit 6 True	76	GND	Ground
37	DB6-	Data Input Bit 6 Complement	77	V_{DD2}	2.5V Power Supply
38	DB5+	Data Input Bit 5 True	78	GND	Ground
39	DB5-	Data Input Bit 5 Complement	79	V_{DD2}	2.5V Power Supply
40	V_{DD1}	3.3V Power Supply	80	SPI_DIS [5]	Serial Port Interface Disable
				EPAD	Analog Ground. Should be connected to ground for electrical and thermal purposes

Note：

1. [1]Nominally 1 kΩ to GND (may be omitted if data clock output is unused).
2. [2] Bypass with 0.1 µF to GND1. Use the buffer amp to drive external circuitry. Limit the output current to 1 µA. Apply an external reference to this pin.
3. [3] Nominally 2 kΩ to GND1 for 20 mA full-scale output (internal reference).
4. [4] If SPI is disabled, tie the pin to V_{DD2} to enable SDR. Otherwise, tie to GND.

5. [5] Tie the pin to V_{DD2} to disable SPI; otherwise, tie to GND.

6. Product Description

6.1 Function Description

The B9726RHQN is a 16-Bit, 400MSPS DAC. The analog supply is 3.3V and digital supply is 2.5V. Data input is low voltage differential signal(LVDS), analog output is single-ended or differential current. An internal precision reference is included.

The B9726RHQN uses LVDS for input data to enable high sample rates and high performance. LVDS technology uses differential signals for noise rejection and small signal amplitude for fast speed with lower power. Each LVDS input on the B9726RHQN has an internal 150Ω active load for proper termination.

Note that in the radiation condition, SPI_DIS should be active high.

6.1.1. DAC Clock And Data Clock Output

The B9726RHQN is used two clock inputs and offers one clock output. All are differential signals.

The B9726RHQN is driven by a master input clock that initiates con-version and controls all on-chip activity. This signal is referred to as the DAC clock. It is not LVDS, and the CLK+ and CLK－ pins are high impedance inputs.

The DAC clock is then used to generate the data clock output. The DCLK_OUT+ and DCLK_OUT－ pins form an LVDS signal that can be used to drive an external FPGA or another data pump. In SDR mode, the data clock output always runs at the same frequency as the DAC clock. In DDR mode, the data clock output always runs at ½ the DAC clock frequency.

Use of the data clock output is optional. It is meant to serve as a convenient means of regulating the incoming data stream. The driver can be loaded by a 100 Ω differential termination. An external 1 kΩ resistor from the REXT pin to DBGND is also required to set the drive strength. If unused, the data clock output pins can be left unconnected, and the 1 kΩ resistor at REXT can be omitted.

6.1.2. Data Clock Input

The remaining clock signal associated with the B9726RHQN is the data clock input (DCLK+, DCLK-). This LVDS signal is not optional and must accompany the

16-bit data bus. The data clock input is used to latch incoming data into the synchronization (sync) logic.

The data clock input always runs at the same frequency as the data clock output in both SDR and DDR modes.

6.1.3. Driving the DAC Clock Inputs

The DAC clock must be precise and spectrally pure to ensure the highest ac performance. A symmetrical 50% duty cycle should be maintained at all times.

The CLK+ and CLK－ input pins should be driven by a signal with a common-mode voltage near ½ of CLKVDD. From this point, peak-to-peak signal amplitude should swing over a range of at least several hundred millivolts.

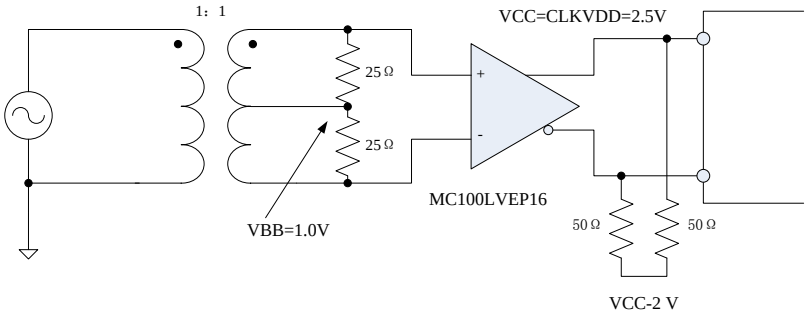


Figure 6-1. Active DAC Clock Driver Circuit

The circuit option shown in Figure 6-1 uses a receiver/driver IC from the 2.5 V LVPECL logic family to provide complementary outputs that fall within these guidelines. A transformer helps ensure a 50% duty cycle and provides a single-ended to differential conversion at the input.

The LVPECL device can be conveniently powered from the same power supply as CLKVDD. The center tap of the transformer secondary must be held at 1 V, the switching threshold of the receiver/driver inputs (use a resistive divider to generate this voltage or use the internal VBB source with a buffer amplifier). Based on a 1:1 impedance ratio, 25Ω resistors across the secondary provide a matched load to a 50 Ω source.

The driver outputs are terminated as close as possible to the B9726RHQN with 50Ω to VCC － 2 V (or use a Thevenin equivalent circuit). Controlled impedance PCB traces should be used to minimize reflections. Signal levels at the CLK+ and CLK－ pins transition between a high near 1500 mV to a low near 750 mV.

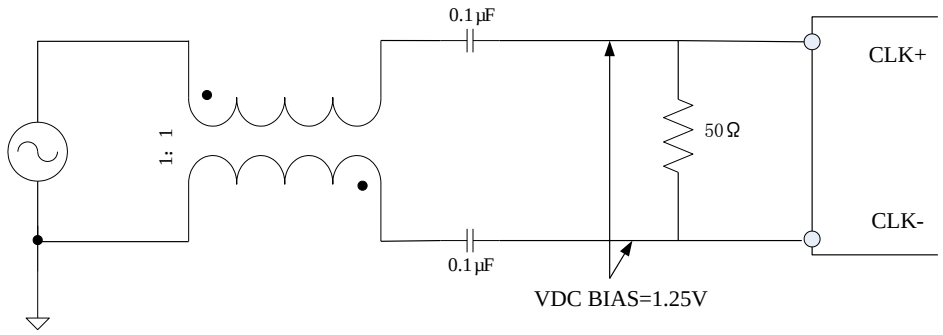


Figure 6-2. Passive DAC Clock Driver Circuit

An alternative circuit option for driving the DAC clock inputs employs a transmission line transformer (balun) to accomplish the single-ended to differential conversion. This all-passive circuit is considerably simpler and less costly, and it provides acceptable performance over a limited range of frequencies.

In this implementation, a sine wave (or other single-ended source) is coupled directly to the differential DAC clock inputs through a 50 Ω transformer. Capacitors are used for isolation, and each DAC clock pin must be dc-biased to a level of 1.25 V (a pair of simple resistive dividers can be used).

The 50Ω termination resistor should be placed as close as possible to the input pins, and controlled impedance PCB traces should be used.

Good ac performance can be expected from either the active or passive DAC clock drive circuit. However, in a passive circuit, the output slew rate is dependent on the frequency of the input; whereas an active circuit provides consistently high output slew rates over a wide range of input frequencies.

6.1.4. Data Synchronization Circuitry

The high performance of the B9726RHQN requires maintaining synchronization between the incoming bits and the DAC clock is used to sample and convert the data. Despite the inherent difficulty in specifying the phase relationship of the DAC clock and the LVDS data clock input and the challenge presented by the high operating speed of the interface, the B9726RHQN contains real-time logic to automatically monitor and align the data bus with the DAC clock.

Whether in SDR or DDR mode, input data is always provided at the same rate. Furthermore, the rate of incoming data always equals the frequency period of the DAC clock. The data rate and the DAC clock must also be frequency locked. To accomplish this, the primary purpose of the data clock output is to provide a time base for data that is derived directly from the DAC clock.

The function of the data clock input is to latch incoming data into the sync block.

From there, it is the function of the synchronization logic to position the data with respect to the DAC clock for optimal ac performance.

Individual data bits must maintain close alignment with one another so that PCB traces have matched delays across the width of the 16-bit bus. In addition, a fixed setup and hold timing relationship between the data clock input and the data bus is required.

However, because of the sync logic, the phase relationship between the data bus and the DAC clock is internally optimized. Furthermore, if the phase between the data bus and the DAC clock drifts over time or temperature, the sync logic automatically updates and adjusts for it. After synchronization is reached, the phase between the data bus and the DAC clock can vary by a full cycle without loss or corruption of data.

More detailed explanations of sync operation and optional programmable modes are presented in the Sync Logic Operation and Programming section, which also includes an explanation of how to use the sync logic without the SPI.

6.1.5. Data Synchronization Circuitry Bypass

Due to internal design limitations, the data synchronization circuitry does not assure a fixed or predictable pipeline delay between the data input and the analog output after power-up. For designs where multichip synchronization or fixed pipeline delay is important, the B9726RHQN can be configured to bypass the resynchronization circuitry and assure a fixed pipeline delay of four DAC clock cycles. In this mode, the data is sampled into the DAC using the DAC clock (CLK±) and following the timing presented in Figure 6-7, Figure 6-8.

The data synchronization circuitry bypass is enabled by writing 0x40 to Address 0x16. The B9726RHQN should also be configured in single data rate mode by writing 0x40 to Address 0x02. In this mode, the sync logic is bypassed, making its configurations and status reporting irrelevant.

6.1.6. Analog Output

The BRHQ9726 is based around a high dynamic range CMOS core. The analog output consists of differential current sources, each capable of up to 20 mA full scale. Discrete output devices are PMOS and capable of sourcing current into an output termination within a compliance voltage range of ±1 V.

In a typical application, both outputs drive discrete resistors-to-analog ground. From there, especially for higher frequency outputs, they feed the center-tap

secondary of a 1:1 RF trans-former. A differential-to-single-ended conversion is accomplished that provides added gain and cancellation of even ordered harmonics.

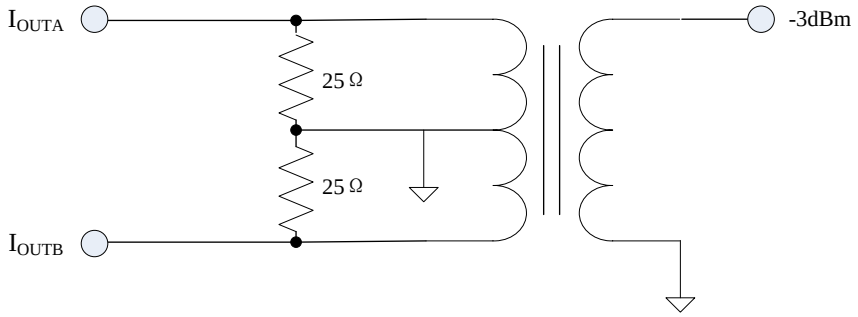


Figure 6-3. Transformer Output Circuit

For maximum output power, resistor values can be increased to 50 Ω to provide up to 0 dBm into a 50 Ω load without loss of performance for most transformers.

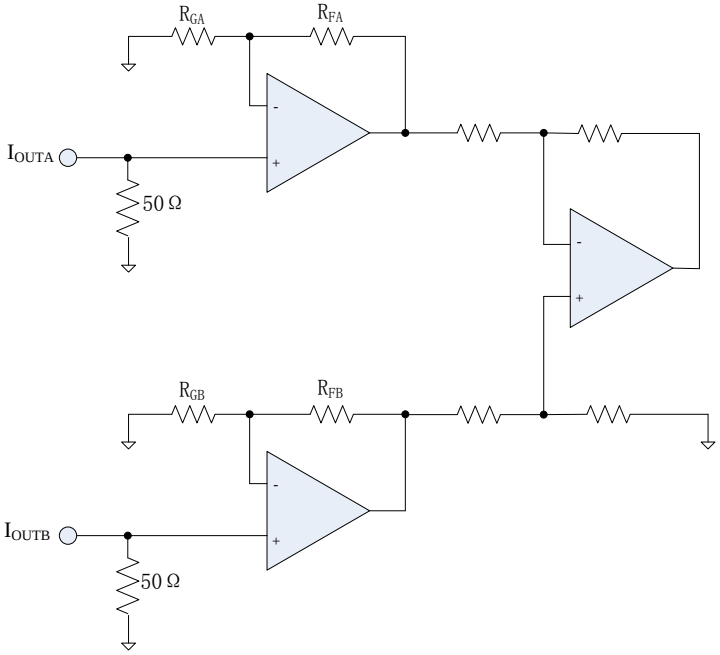


Figure 6-4. Op Amp Output Circuit

As an alternative, an active output stage can be used in the classic instrumentation amplifier configuration. Here, each DAC output feeds the non-inverting input of one of the Analog Devices, Inc., high speed trans impedance op amps.

6.1.7. Internal Reference And Full-Scale Output

The B9726RHQN contains an internal 1.2 V precision reference source; this reference voltage appears at the REFIO pin. It can be used to drive external circuitry if properly buffered.

Apply an external reference voltage source to the REFIO pin if desired. The internal source is designed to be easily overdriven by an external source; however, the internal reference can also be powered down using the EXTREF bit in SPI Register 0x00.

The reference voltage (either internal or external) is applied to an external precision resistor at the FSADJ pin. The resulting current is internally amplified to provide the full-scale current at the DAC output according to the following equation:

$$I_{OUTFS} = VREF / R_{FSADJ} \times 32$$

Taking into account the binary value appearing at the data bus inputs, the output currents IOUTA and IOUTB can be determined according to the following equations:

$$I_{OUTA} = I_{OUTFS} \times DB[15:0] / 65536$$

$$I_{OUTB} = I_{OUTFS} \times (65535 - DB[15:0]) / 65536$$

Note that the B9726RHQN features nonvolatile, factory-calibrated gain using the internal reference source and a precision 2 kΩ load. Gain accuracy in any application is, therefore, dependent upon the accuracy of R_{FSADJ}.

Table 6-1 shows the relationship between straight binary and twos complements binary.

Table 6-1. straight binary and twos complements binary

straight binary		twos complements binary		IOUTA Output Current
Binary（DB[15：0]）	Decimal	Binary（DB[15：0]）	Decimal	
1111 1111 1111 1111	65535	0111 1111 1111 1111	32767	I_{OUTFS}x65535/65536
1111 1111 1111 1110	65534	0111 1111 1111 1110	32766	I_{OUTFS}x65534/65536
⋮	⋮	⋮	⋮	⋮
1000 0000 0000 0001	32769	0000 0000 0000 0001	1	I_{OUTFS}x32769/65536
1000 0000 0000 0000	32768	0000 0000 0000 0000	0	I_{OUTFS}x32768/65536
0111 1111 1111 1111	32767	1111 1111 1111 1111	-1	I_{OUTFS}x32767/65536
⋮	⋮	⋮	⋮	⋮
0000 0000 0000 0001	1	0000 0000 0000 0001	-32767	I_{OUTFS}x1/65536
0000 0000 0000 0000	0	1000 0000 0000 0000	-32768	0

6.1.8. RESET

Following initial power-up and application of a valid DAC clock signal, the B9726RHQN should always be initialized with an active high pulse on the RESET pin. This defaults the programmable registers, initializes volatile calibration memory, and prepares the synchronization logic for data. The data bus should be static prior to

the reset pulse. After reset, LVDS data can flow.

The default state of the B9726RHQN is DDR and twos complement binary input data. To use the B9726RHQN in this mode, it is not necessary to program any device registers. However, the SPI is enabled by default unless the SPI_DIS pin is connected high. If not disabled, SPI input pins should not be left floating.

6.1.9. SPI Register Description

Table 6-2. SPI Register Map

addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0X00	SDDIR	DADIR	SWRET	SLEEP	PWDN			EXTREF
0X02	DAFMT	DARAT	IDKI	IDKO	DISDKO	SYNMA	SYNPD	SYNRM
0X0E			CALMM[1]	CALMM[0]		CALCK[2]	CALCK[1]	CALCK[0]
0X0F	SCATAT	SELCAL	XFETAT	MMFER	SMWR	SMRD	FMRD	UNCAL
0X10	MMDR[7]	MMDR[6]	MMDR[5]	MMDR[4]	MMDR[3]	MMDR[2]	MMDR[1]	MMDR[0]
0X11			MMDT[5]	MMDT[4]	MMDT[3]	MMDT[2]	MMDT[1]	MMDT[0]
0X15							SYNOUT[1]	SYNOUT[0]
0X16			SYNEXT	SYNIN[1]	SYNIN[0]			

Table 6-3. SPI Register Bit Default and Description Values

addr	name	Bit	I/O	default	description
0x00	SDDIR	7	I	0	0: SDIO is input only (4-wire SPI mode), and SDO is used for output. 1: SDIO is input/output (3-wire SPI mode), and SDO is unused.
	DADIR	6	I	0	0: SPI serial data byte is MSB first format. 1: SPI serial data byte is LSB first format.
	SWRET	5	I	0	1: software reset: SPI registers (except 0x00) to default values.
	SLEEP	4	I	0	1: analog outputs temporarily disabled.
	PWDN	3	I	0	1: full device power-down; all circuits disabled except SPI.
	EXREF	0	I	0	1: power-down internal reference; use external reference source.
0x02	DAFMT	7	I	0	0: input data-word is twos complement binary format. 1: input data-word is unsigned binary format.
	DARAT	6	I	0	0: DDR mode. 1: SDR mode.
	IDKI	5	I	0	1: inverts the polarity of the data clock input.
	IDKO	4	I	0	1: inverts the polarity of the data clock output.
	DISDKO	3	I	0	1: disables the data clock output.
	SYNMA	2	I	0	1: enables sync manual mode; disables automatic update.
	SYNPD	1	I	0	1: forces manual sync update.
	SYNRM	0	O	0	1: indicates that sync logic requires update.

0x0E	CALMM	[5:4]	O	00	2-bit SMEM contents and calibration status indicator. 00: uncalibrated; SMEM contains default values (63). 01: self-calibrated; SMEM contains values from self-calibration. 10: factory-calibrated; SMEM values are transferred from FMEM. 11: user-calibrated; SMEM contains user-entered values.
	CALCK	[2:0]	I	000	3-bit self-calibration clock divider ratio. 000: self-calibration clock is DAC clock/4096. 001,010,011: self-calibration clock is DAC clock/2048,1024,512. 100,101,110: self-calibration clock is DAC clock/256,128,64. 111: self-calibration clock is DAC clock/32
0x0F	SCATAT	7	O	0	1: indicates completion of self-calibration cycle.
	SELCAL	6	I	0	1: initiates self-calibration cycle.
	XFETAT	5	O	0	1: indicates completion of memory transfer cycle.
	MMFER	4	I	0	1: initiates FMEM to SMEM transfer
	SMWR	3	I	0	1: enables static memory (SMEM) write operation.
	SMRD	2	I	0	1: enable static memory (SMEM) read operation.
	FMRD	1	I	0	1: enables factory memory (FMEM) read operation.
	UNCAL	0	I	0	1: enables uncalibrated operation; all SMEM to default values.
0x10	MMDR	[7:0]	I	00000000	8-bit memory address value for read/write operations.
0x11	MMDT	[5:0]	I/O	000000	6-bit memory data value for read/write operations
0x15	SYNOUT	[1:0]	O	00	2-bit output value indicates current sync quadrant
0x16	BYPASS	6	I	0	1: bypasses data synchronization circuitry. Data is sampled using the DAC clock (CLK±)
	SYNEXT	5	I	0	1: enables sync external mode; disable auto quadrant select.
	SYNIN	[4:3]	I	00	2-bit input value is used to specify the sync quadrant.

6.1.10. Timing Diagrams

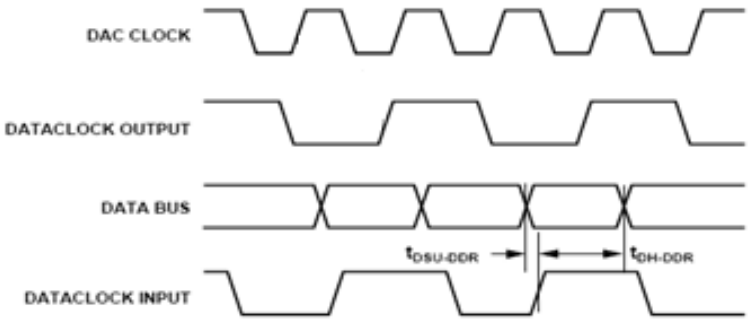


Figure 6-5. DDR Timing Diagram

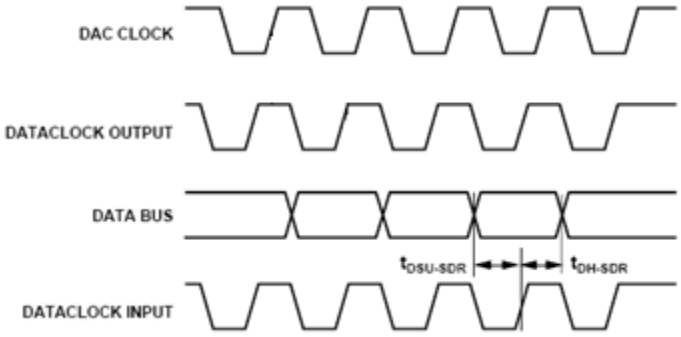


Figure 6-6 SDR Timing Diagram

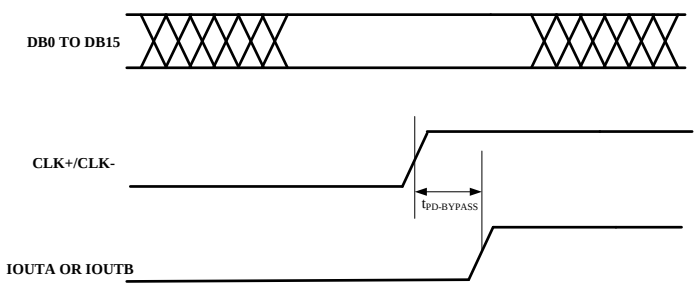


Figure 6-7 Data Synchronization Timing Diagram

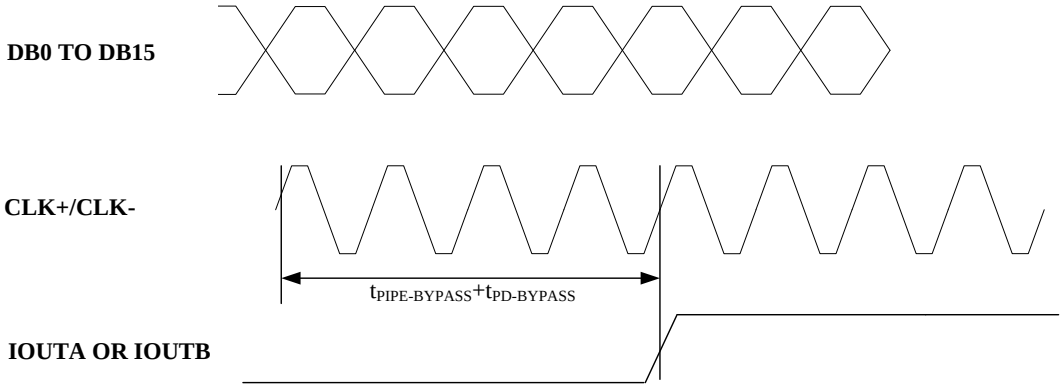


Figure 6-8 Data Synchronization Bypass Pipeline Delay

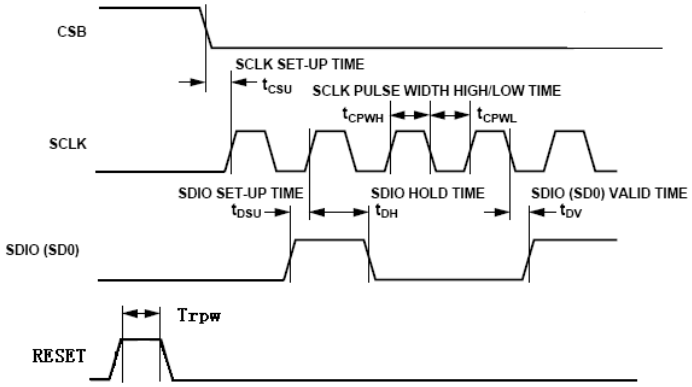


Figure 6-9 SPI Timing Diagram

6.1.11. Timing Specifications

V_{DD1}=3.3V,V_{DD2}= 2.5V, Io=20mA, internal reference, unless otherwise specified.

Table 6-4. Timing Specification

Parameter	Symbol	Conditions V_{DD1}=3.3V, V_{DD2}=2.5V Io=20mA ，-55℃ ≤ T_A≤ 125℃	Values			Units
			Min.	Typ.	Max.	
DDR DB[15:0]± Setup Time	$t_{DSU-DDR}$		0.5	—	—	ns
DDR DB[15:0]± Hold Time	t_{DH-DDR}		0.5	2.5	—	ns
SDR DB[15:0]± Setup Time	$t_{DSU-SDR}$		0.5	—	—	ns
SDR DB[15:0]± Hole Time	t_{DH-SDR}		0.5	1.2	—	ns
CLK± to IOUT Propagation Delay	$t_{PD-BYPASS}$		—	0.85	—	ns
DB[15:0]± to IOUT Pipeline Delay	$t_{PIPE-BYPASS}$		—	4	—	DAC clock cycles
SCLK Frequency	f_{SCLK}		—	—	15	MHz
SCLK Pulse Width High	t_{CPWH}		33	—	—	ns
SCLK Pulse Width Low	t_{CPWL}		33	—	—	ns
SCLK Setup Time	t_{CSU}		33	—	—	ns
SDIO Setup Time	t_{DSU}		33	—	—	ns
SDIO Hold Time	t_{DH}		0	66	—	ns
SDIO/SDO Valid Time	t_{DV}		—	60	—	ns
RESET Pulse Width			5	—	—	ns

6.1.12. SPI Configuration Description

The serial port interface is a flexible and synchronous serial communications port allowing easy interface to many industry standard microcontroller and microprocessor protocols (including both Motorola SPI and Intel SSR). The interface provides read/write access to registers that configure the operation of the B9726RHQN.

The B9726RHQN SPI supports single-byte and multibyte transfers as well as MSB- or LSB-justified data formats. The interface can be configured in 3-wire mode (in which SDIO is bidirectional) or the default 4-wire mode (in which SDIO and SDO function as unidirectional data input and data output, respectively).

Communication Cycle

All communication cycles have two phases. The first phase is concerned with

writing an instruction byte into the SPI controller and always coincides with the first eight rising edges of SCLK. The instruction byte provides the controller with information regarding the second phase of the cycle, namely the data transfer phase. The instruction byte contains the number of data bytes to be transferred (one to four), a register address, and a bit initiating a read or write operation.

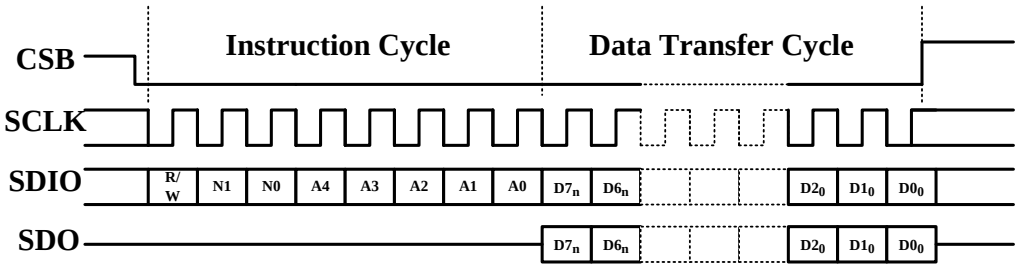


Figure 6-10. SPI Communication Cycle

Any communication cycle begins with CSB going low, which also resets the SPI control logic. Similarly, any communication cycle ends with CSB going high, which aborts any incomplete data transfer. After a communication cycle begins, the next eight SCLK rising edges interpret data on the SDIO pin as the instruction byte.

Instruction Byte

The instruction byte bits are shown in the following bit map.

Table 6-5. Instruction Byte Bits Map

B7	B6	B5	B4	B3	B2	B1	B0
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$

Bit 7 of the instruction byte selects a read or write transfer. If the bit is set high, a read operation is indicated. If the bit is low, a write operation is indicated.

N1，N0

Bit 6 and Bit 5 of the instruction byte determine the number of data bytes to be transferred, as shown in Table 6-6.

Table 6-6. The Number of Data Bytes

N1	N0	Description
0	0	Transfer one data byte
0	1	Transfer two data byte
1	0	Transfer three data byte
1	1	Transfer four data byte

A4，A3，A2，A1，A0

Bit 4 through Bit 0 of the instruction byte specify a 5-bit binary value corresponding to a valid register address. In the case of multibyte transfers, the

location specified is either an initial or a concluding register address. The SPI controller increments or decrements this value to generate successive address values depending on whether LSB or MSB justification is active.

MSB/LSB Transfers

The SPI can support both MSB- and LSB-justified serial data byte formats. This functionality is determined by Bit 6 in SPI Register 0x00. This bit defaults low, which is MSB justification. In this mode, serial data bits are written to and/or read from registers sequentially from Bit 7 to Bit 0.

If Bit 6 of SPI Register 0x00 is set high, the controller switches to LSB justification. In this mode, data bits are written to or read from registers sequentially from Bit 0 to Bit 7. Writing to the instruction bytes is also affected by the active justification.

For multi-byte transfers with MSB justification, the address in the instruction byte is interpreted as a final address, and its value is decremented automatically by the controller. For multi-byte transfers with LSB justification, the address in the instruction byte is interpreted as an initial address, and its value is incremented automatically by the controller.

Care must be exercised when switching from MSB to LSB justification. The controller switches modes immediately once all eight bits of SPI Register 0x00 are written (even if in the process of a multi-byte transfer). For this reason, a single byte command is recommended when changing justification.

3-Wire and 4-Wire Operation

Bit 7 of SPI Register 0x00 defaults low, enabling 4-wire SPI operation. In this mode, serial data is input from the SDIO pin, and serial data is output on the SDO pin. Setting Bit 7 of SPI Register 0x00 high enables 3-wire operation. In this mode, SDIO becomes bidirectional and switches automatically from input to output when necessary. The SDO pin in this mode is unused and assumes a high impedance state.

As with MSB or LSB justification, care must be exercised when switching operational modes. The change occurs immediately once all eight bits of SPI Register 0x00 are written.

Writing and Reading Register Data

Bringing CSB low initiates a new communication cycle. The next eight rising edges of SCLK latch data from SDIO into the instruction byte. If Bit 7 of the instruction byte is low, a write operation is enabled. If Bit 7 is high, a read operation is enabled.

For a write operation, a data byte is latched from the SDIO pin into a register on the next eight rising edges of SCLK. If the instruction byte Bit 6 and Bit 5 are not both 0, a multibyte transfer latches data bytes into adjacent registers after each successive set of eight rising SCLK edges. Depending upon MSB or LSB justification, the controller decrements or increments the address value in the instruction byte during the cycle as necessary.

If a read operation is enabled, data bits from the register being addressed appear on SDO (or SDIO) with each falling edge of SCLK. Note that for a read operation, the eighth bit of the instruction byte is latched on the eighth rising edge of SCLK, and the first output bit is enabled on the immediately following falling SCLK edge.

For multi-byte read sequences, the controller adjusts the register address when necessary, and subsequent data bit values appear at the output with each falling SCLK edge.

Disabling the SPI

Tie the SPI_DIS pin high to ADVDD to disable the serial port interface. In this state, the default DDR operational mode can be changed to SDR by pulling the SDR_EN pin high to ADVDD. In addition, with the SPI disabled, the sync logic no longer operates in a fully automatic mode. See the Sync Logic Operation and Programming section for a full explanation of sync operational modes.

Note that in the radiation condition, SPI_DIS should be active high.

6.1.13.SPI Pin Description

The B9726RHQN SPI logic input/output thresholds are based upon a nominal 3.3 V level. The maximum frequency of operation is 15 MHz.

Chip Select (CSB)

The CSB pin is an active low input. It begins and ends any communication cycle and must remain low during the entire cycle. An incomplete cycle is aborted if CSB is prematurely returned high.

Serial Clock (SCLK)

The SCLK pin is used to synchronize data to and from the SPI registers, and the controller state machine runs from this input. It is, therefore, possible to read and write register data (but not SMEM/FMEM) without a valid DAC clock. All input data is registered on the rising edge of SCLK, and output data bits are enabled on the falling edge of SCLK.

Serial Data Input/Output (SDIO)

Data is always written into the SPI on the SDIO pin. In 3-wire mode, however, data is also driven out using this pin. The switch from input to output occurs automatically between the instruction and data transfer phases of a read operation. In the default 4-wire mode, SDIO is unidirectional and input only.

Serial Data Output (SDO)

Serial data is driven out on the SDO pin when the SPI is in its default 4-wire mode. In 3-wire mode (or whenever CSB is high), SDO is set to a high impedance state.

6.1.14.Self-Calibration

The B9726RHQN features an internal self-calibration engine to linearize the transfer function automatically. This can be very useful at temperature extremes where factory calibration no longer applies. The automated cycle can be initiated by asserting the SELFCAL bit.

The self-calibration process calibrates all linearity and gain CALDACs based upon a fixed internal reference current. Values for all CALDACs are stored in volatile static memory. The SCATAT bit indicates the successful completion of the cycle, and the SELFCAL bit is cleared. Following the cycle, the device reports a self-calibrated state (CALMEM = 01b).

Table 6-7. SPI Configuration about Self-Calibration

0x0E	CALMM	[5:4]	O	00	2-bit SMEM contents and calibration status indicator. 01: self-calibrated; SMEM contains values from self-calibration.
	CALCK	[2:0]	I	000	3-bit self-calibration clock divider ratio. 000: self-calibration clock is DAC clock/4096. 001,010,011: self-calibration clock is DAC clock/2048, 1024,512. 100,101,110: self-calibration clock is DAC clock/256,128,64. 111: self-calibration clock is DAC clock/32
0x0F	SCATAT	7	O	0	1: indicates completion of self-calibration cycle.
	SELCAL	6	I	0	1: initiates self-calibration cycle.

When successful assertion of the SELFCAL bit (Bit 6 in Register 0x0F) requires that Bits[5:0] in Register 0x0F be clear. If any of these bits are asserted, the self-calibration cycle does not begin.

The time required to self-calibrate is dependent on both the DAC clock frequency and the value of CALCLK (Bits[5:0] in Register 0x0E). Because self-calibration requires more time than ordinary operation, the DAC clock is divided

into a slower version and used to step through the process. Time made available to the self-calibration algorithm directly impacts its ability to provide accurate results.

A maximum fixed division ratio (4096) corresponds to the minimum default value of CALCLK (0). The division ratio can be decreased by increasing the value of CALCLK. Each increase in the value of CALCLK reduces the DAC clock division factor (and, therefore, the time made available to self-calibration) by 50%. With CALCLK at its maximum value (7), the divide ratio declines to its minimum value (32).

With CALCLK at its default value, self-calibration requires approximately 100 ms at a DAC clock frequency of 100 MHz. This time can be reduced to under 0.8 ms if CALCLK = 7. Time scales relative to DAC clock frequency.

6.1.15. SYNC Logic Operation and Programming

Recall that a fixed setup and hold timing relationship between the data clock input and the data bus must be established and maintained. Recall also that the data bus and the DAC clock must be frequency locked. Because of the sync logic, however, the phase relationship between the data bus and the DAC clock is internally optimized. Therefore, data arrival propagation delays and concern about data transitions near the sampling instant are eliminated.

Synchronization is automatically enabled upon reset. After data arrives and synchronization is achieved, the sync logic continuously monitors itself so that automatic adjustments are made if phase drifts occur over time and/or temperature.

Note that the sync function and operation of the sync logic block are transparent, automatic, and ongoing. No programming is required. For applications where it is useful, however, the following programmable control is provided.

SYNC Operating States

The sync logic can operate in one of three possible modes. The default mode is fully automatic.

Fully automatic synchronization is accomplished by demultiplexing the incoming data stream into four channels, each containing every fourth data-word. Data-words are present for four DAC clock cycles. Data is remultiplexed by sampling each channel with the optimum DAC clock cycle.

Initial synchronization is first established through a hardware reset. This also fully enables the synchronization logic to monitor and resynchronize, as necessary. The B9726RHQN resynchronizes only if conditions change enough to alter the phase

between the data bus and the DAC clock by more than one full clock cycle. In this event, an internal alarm occurs and is followed by an automatic update. During resynchronization, two data-words are typically lost or repeated.

In addition to fully automatic mode, two semi-automatic modes are available.

Sync Manual Mode

In fully automatic mode, the B9726RHQN both detects when a resynchronization is necessary and initiates an update. In manual mode, automatic updating is disabled. Enable manual mode by setting the SYNCMAN bit in SPI Register 0x02.

In manual mode, the sync logic still monitors incoming data and the DAC clock, but it indicates the need for an update by asserting the SYNRM bit (Bit 0 in Register 0x02). In this mode, the user is expected to regularly poll the SYNRM bit. When this bit is read back high, the user can issue a manual sync update also by asserting the SYNPD bit (Bit 1) in SPI Register 0x02.

SYNRM does not indicate that data is being lost but that conditions are close to the point where data may be lost. The sync logic should be resynchronized by asserting SYNPD at the next convenient time.

In manual mode, users can choose when to update the sync logic. When operating with burst data, issuing a sync update between active bursts updates the system without risking the loss of any data. In fact, because SYNPD always forces a resynchronization regardless of operational mode, even users in fully automatic mode can reduce the possibility of data loss by occasionally forcing a sync update during idle activity.

If either the data clock or the DAC clock is interrupted for any reason, a SYNPD should always be executed to ensure that data bus and DAC clock phase alignment remains optimized.

SYNC External Mode

Going beyond manual mode, sync external mode offers a greater level of control and can be useful if multiple DAC channels are employed in an application. Enable sync external mode by asserting the SYNEXT bit (Bit 5) in SPI Register 0x16. Manual mode must also be enabled.

The four channels into which each incoming data-word is multiplexed are called quadrants. In any mode, the current quadrant value can always be read back via SYNOUT (Bits [1:0] of SPI Register 0x15). At sync update, the logic chooses the optimal quadrant and refreshes the value of SYNOUT.

It is also possible to enter a value into SYNIN (Bits [4:3] of SPI Register 0x16). When external mode is enabled, the logic operates as expected, except that the quadrant value in SYNIN is used following an update. This can be used to align delays between multiple device outputs.

6.2 Storage Condition

The warehouse environment of B9726RHQN should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

Table 6-8. The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

6.3 Absolute maximum ratings

a) Power Supply（V_{DD1}）…… -0.3V～+3.6V

b) Power Supply（V_{DD2}）…… -0.3V～+2.8V

c) Clock Input Voltage（V_{CLK+}，V_{CLK-}）…… -0.3V～V_{DD2} +0.3V

d) Input Voltage:

（$V_{DB[15:0]+/-}$,$V_{DCLK\_IN+/-}$,$V_{DCLK\_OUT+/-}$) …… -0.3V～V_{DD1} +0.3V

（V_{CSB}，V_{SCLK}，V_{SDIO}，V_{SDO}，V_{RESET}，V_{REXT}) …… -0.3V～V_{DD1} +0.3V

（V_{REFIO}，V_{FSADJ}）…… -0.3V～V_{DD1}+0.3V

（V_{SDR_EN}，V_{SPI_DIS}）…… -0.3V～V_{DD2} +0.3V

e) Power Dissipation（TA ≤ 125 ℃）…… 2.0W

f) Storage Temperature (T_{STG}) …… -65℃～+150℃

g) Weld Temperature（10s）(T_h) …… 260 ℃（Mac.），300 ℃（Manual）

h) Thermal Resistance（$R_{th(J-C)}$）…… 5.0℃/W

i) Junction Temperature（T_J）…… 175℃

6.4 Recommended operating conditions

a) Power Supply（V_{DD1}）…… +3.13 V～+3.47 V

b) Power Supply（V_{DD2}）…… +2.37 V～+2.63 V

c) Ambient Temperature Range（T_A）…… -55℃～+125℃

6.5 Radiation hardened performance

a) Total Ionizing Dose ≥ 100 Krad(Si)

b) SEL threshold ≥ 75 MeV cm^2/mg

7. Electrical Characteristic

V_{DD1}=3.3V，V_{DD2}= 2.5V，Io=20mA，internal reference, unless otherwise specified.

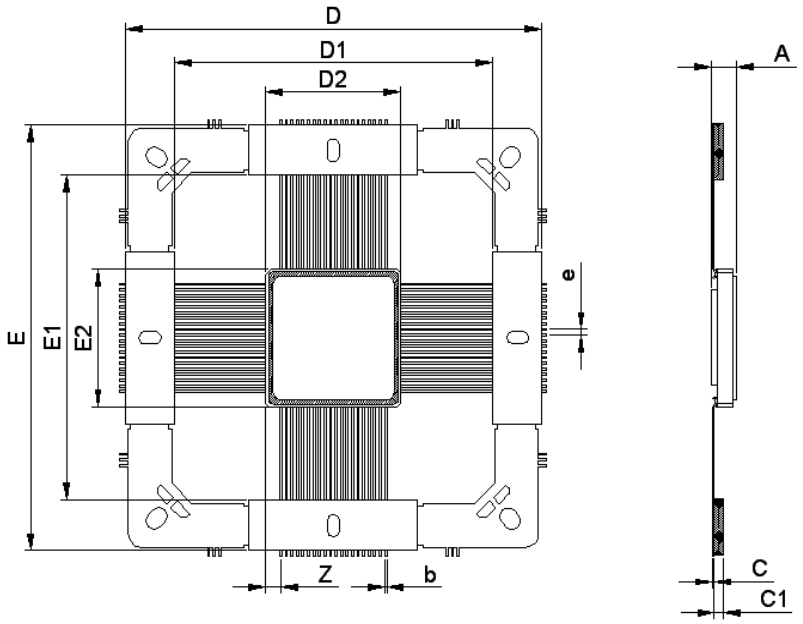
Table 7-1. Electrical Characteristic

Parameter	Symbol	Conditions V_{DD1}=3.3V，V_{DD2}=2.5V Io=20mA ，-55℃ ≤ T_A≤ 125℃	Values		Units
			Min.	Max.	
Resolution	*RES*		16	—	Bits
Differential Non-Linearity	E_{DL}	Differential Output，External Reference	-4.0	+4.0	LSB
Integral Non-Linearity	E_L	Differential Output，External Reference	-9.0	+9.0	LSB
Offset Error	E_O		-2. 0	+2. 0	%FS
Gain Error	E_G		-2.0	+2.0	%FS
Reference Output Voltage	V_{REF}		1.14	1.42	V
3.3V Supply Current	I_{DD1}	f_{CLK}=100MSPS，f_O=1.0MHz	—	400.0	mA
2.5V Supply Current	I_{DD2}	f_{CLK}=100MSPS，f_O=1.0MHz	—	220.0	mA
Clock Differential Input Voltage	V_{DCLK}	CLK+/-	0.5	—	V
Clock Input Common Voltage	V_{CCLK}		1.0	—	V
CMOS Input High Level	V_{IH}	CSB,SCLK,SDIO,RESET	2.5	—	V
CMOS Input Low Level	V_{IL}		—	0.5	V
CMOS Output High Level	V_{OH}	SDO	3.0	—	V
CMOS Output Low Level	V_{OL}		—	0.6	V
Control Input High Level	V_{ICH}	SPI_DIS,SDR_EN	2.0	—	V
Control Input Low Level	V_{ICL}		—	0.5	V
High Level Input Current	I_{IH}	SPI_DIS,SDR_EN，V_{IH}=2.5V	-10	+10	uA
Low Level Input Current	I_{IL}	SPI_DIS,SDR_EN，V_{IH}=0V	-10	+10	uA
Spurious-Free dynamic Range	*SFDR*	f_{CLK}=200MSPS，f_O=1MHz，R_l=25Ω	72	—	dBc
		f_{CLK}=200MSPS，f_O=2MHz，R_l=25Ω	70	—	
		f_{CLK}=400MSPS，f_O=1MHz，R_l=25Ω	68	—	
		f_{CLK}=400MSPS，f_O=2MHz，R_l=25Ω	66	—	
Total Harmonic Distortion	*THD*	f_{CLK}=400MSPS，f_O=1MHz，R_l=25Ω	—	-66	dBc

8. Typical Application（Appendix Ⅰ）

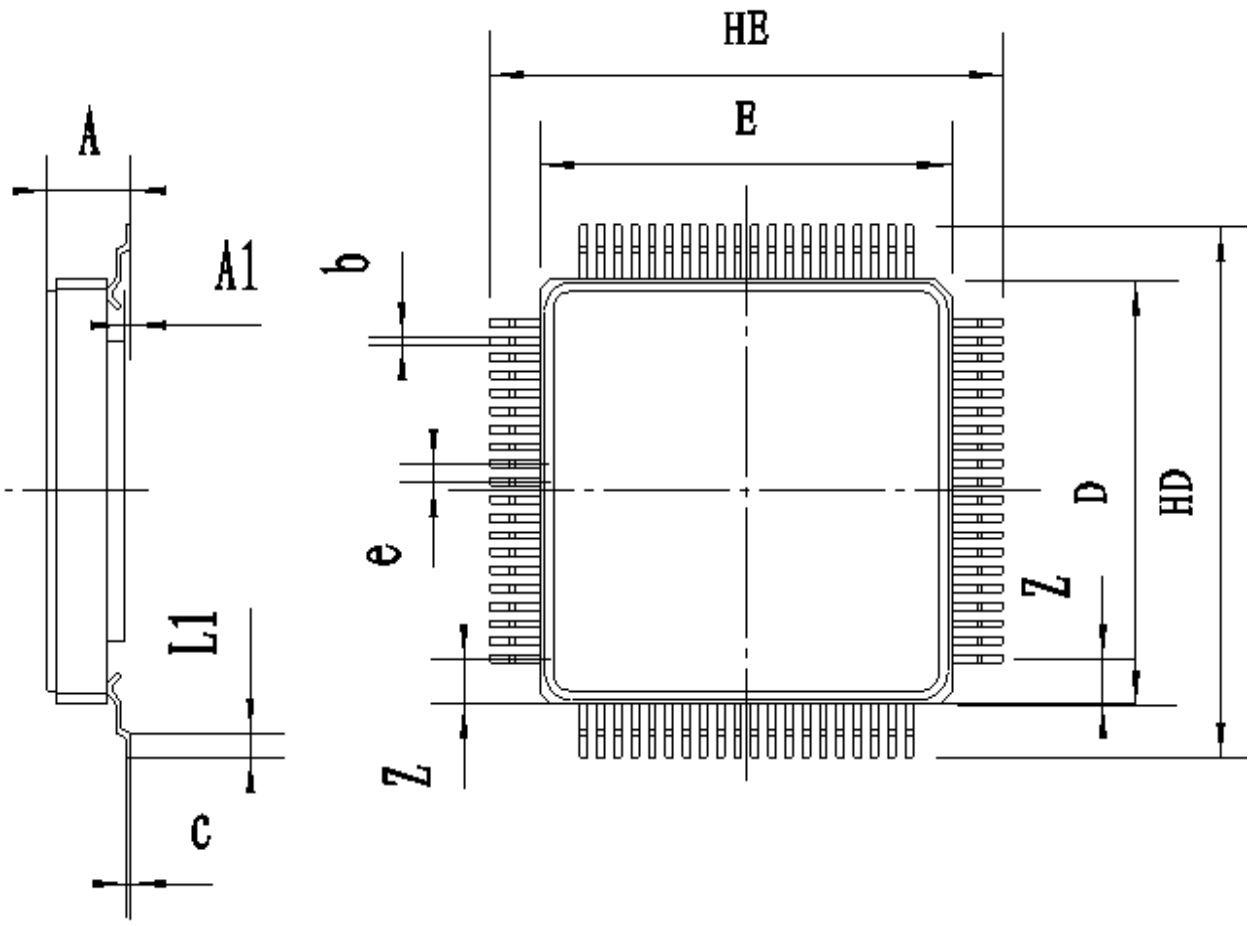
9. Package Outline Dimensions

B9726RHQN's package style is CQFP80, its physical size is shown in figure9-1.



Symbol	Values(Units: mm)		
	Min.	Typ.	Max.
A	1.85	—	2.95
b	0.12	—	0.28
c	0.07	—	0.23
c1	0.66	—	1.12
D/E	36.85	—	38.05
D1/E1	27.26	—	29.86
D2/E2	11.70	—	12.30
e	—	0.50	—
Z	1.11	—	1.39

Figure 9-1. Physical Dimension



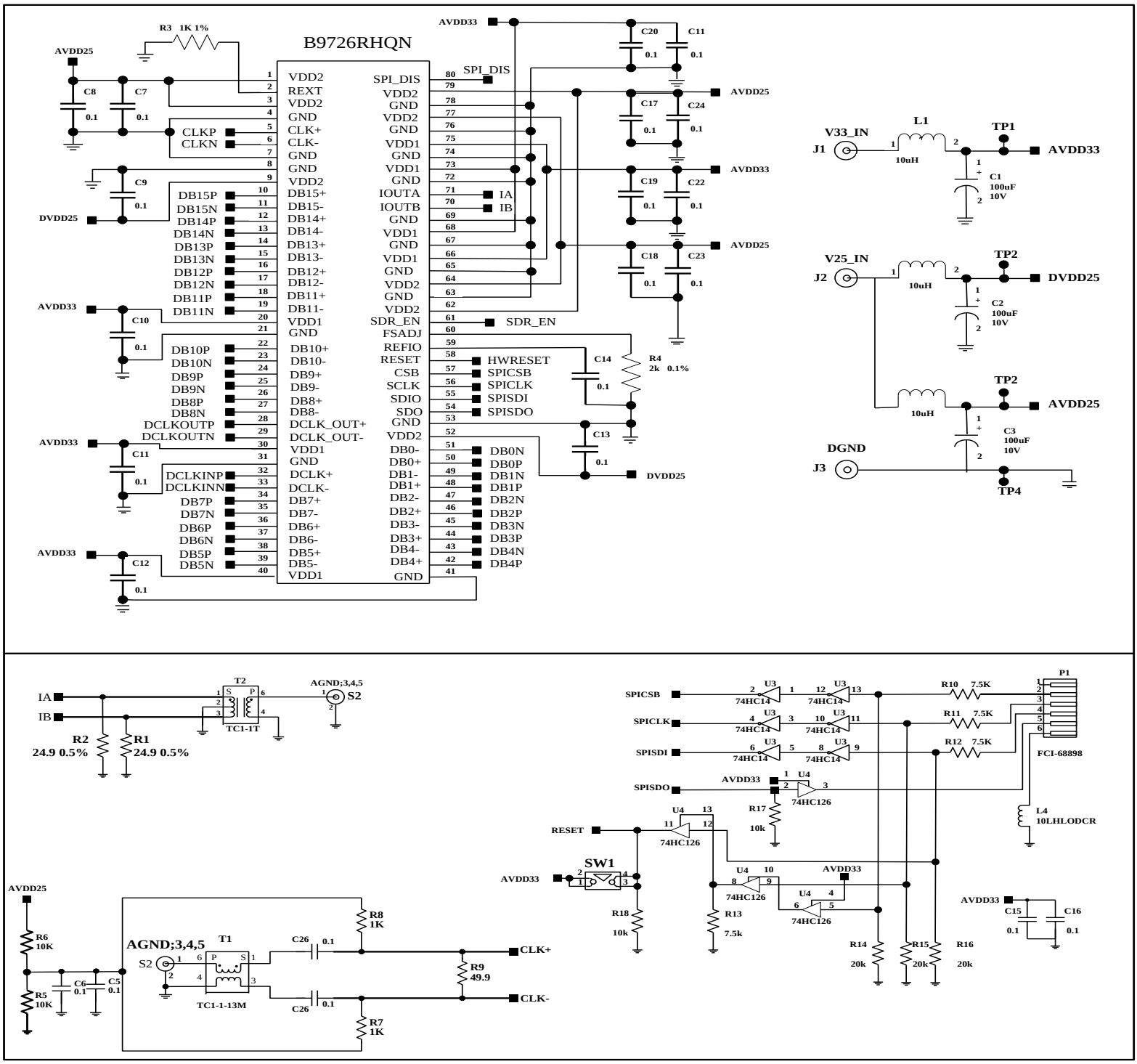
Symbol	Values（Units:mm）		
	Min.	Typ.	Max.
A	2.5	___	3.5
A1	0.5	___	1.01
b	___	0.22	___
c	___	0.15	___
e	___	0.5	___
Z	___	1.25	___
D/E	11.85	12	12.15
HD/HE	15.95	17	17.65
L1	1.25	1.5	1.75

Appendix Ⅰ Typical Application

Applications

Instrumentation ,Test equipment ,Waveform synthesis , Communications systems.

Evaluation Board



App. Evaluation Board

Service & Supply

Address：No.2.Siyingmen N.Rd.Donggaodi, Fengtai District, Beijing, PRC

Department：Department of international cooperation

Telephone：010-67968115-8334

Fax：010-68757706

Zip code：100076