Ver 1.1

12-Bit 120MSPS Digital to Analog Converter

Datasheet

Part Number：B9762AMG

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1. Features

- 120 MSPS Update Rate
- 12-Bit Resolution
- Excellent Spurious Free Dynamic Range Performance
- Differential Current Outputs: 2 mA to 20 mA
- Power Dissipation: 220 mW @ 5 V
- Single +5 V or +3 V Supply Operation
- Package: 28-Pin CPGA
- Edge-Triggered Latches

2. Product Description

The B9762AMG is a radiation hardened, 12-bit resolution chip, low power CMOS digital-to-analog converters (DACs). It is specifically optimized for the transmit signal path of communication systems. The B9762AMG offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The B9762AMG's flexible single-supply operating of 3.3 or 5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a half with a slight degradation in performance by lowering the full-scale current output.

The B9762AMG is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3.3 V or +5 V CMOS logic families.

The B9762AMG is a current-output DAC with a nominal full-scale output current of 20mA .

Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The B9762AMG can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier, which provides a

wide (>10:1) adjustment span, allows the B9762AMG full-scale current to be adjusted over a 2mA to 20mA range while maintaining excellent dynamic performance. Thus, the B9762AMG may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The B9762AMG is available in a 28-lead CPGA package. It is specified for operation over the industrial temperature range.

3. Functional Block Diagram

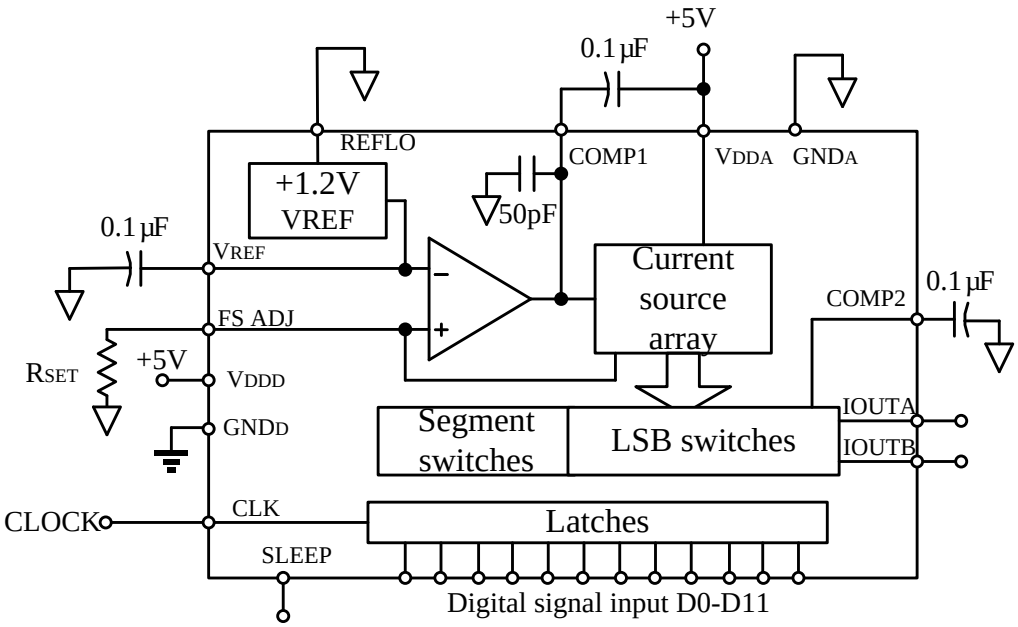


Figure 3-1. Functional Block Diagram

4. Pin Description

CPGA28 Packaging,

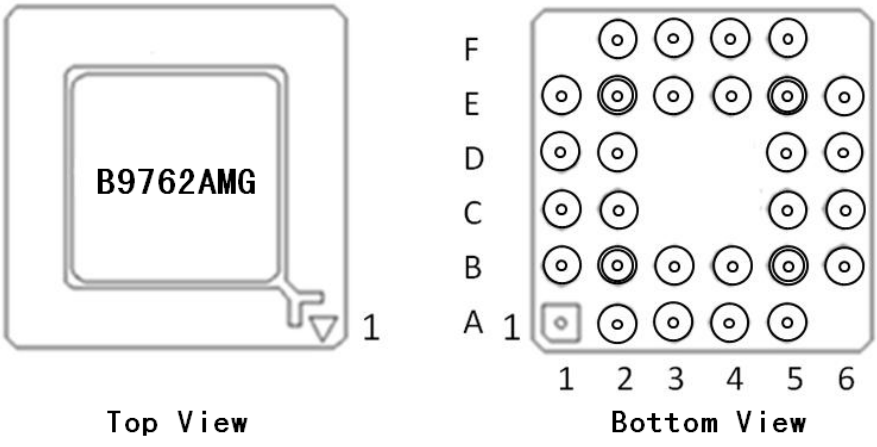


Figure 4-1, Pin Description

Table 4-1 B9762AMG Pin Description

Symbol	Function Description
D0~11	Data Bits（LSB~MSB）
SLEEP	Power Down Control Input, HI：Sleep, LO：Normal
REFLO	Reference choose. 1) Connect to VDDA to disable internal reference . 2)Ground when Internal 1.2 V Reference Used.
V_{REF}	Reference Input/Output
FSADJ	Full-Scale Current Output Adjust
COMP1	Bandwidth/Noise Reduction Node. Add 0.1 mF to VDDA for optimum performance
GND_A	Analog Common.
IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
COMP2	Internal Bias Node for Switch Driver Circuitry. Decouple to GND with 0.1 mF capacitor
V_{DDA}	Analog Supply Voltage
GND_D	Digital Common.
V_{DDD}	Digital Supply Voltage (+5 V).
CLK	Clock Input. Data latched on positive edge of clock
NC	No Connect

Note：All input pins are should not float.

5. Pin Definition（Appendix 1）

6. Product Highlights

1. Manufactured on a CMOS process, the B9762AMG own high performance.

2. On-chip, edge-triggered input CMOS latches readily interface to +3.3 V and +5 V CMOS logic families. The B9762AMG can support update rates up to 120 MSPS.

3. A flexible single-supply operating range of 3.3V or 5.5V, and a wide full-scale current adjustment span of 2mA to 20mA, allows the B9762AMG to operate at reduced power levels.

4. The current output(s) of the B9762AMG can be easily configured for various

single-ended or differential circuit topologies.

7. Production Application

7.1 Functional Description

Figure 7-1 shows a simplified block diagram of the B9762AMG. The B9762AMG consists of a large PMOS current source array that is capable of providing up to 20 mA of total current. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance.

All of these current sources are switched to one or the other of the two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The analog and digital sections of the B9762AMG have separate power supply inputs (i.e., V_{DDA} and V_{DDD}) that can operate independently over a 3.3 volt or 5 volt range. The digital section, which is capable of operating up to a 120 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2mA to 20mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is 32 times the value of I_{REF}.

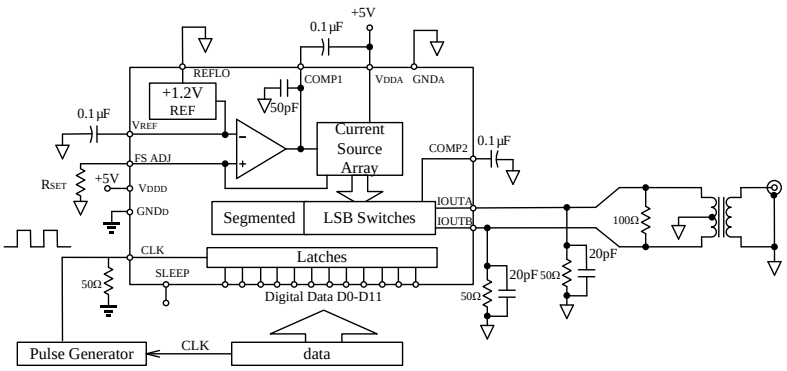


Figure 7-1. Basic AC Characterization Test Setup

7.1.1 Dac Transfer Function

The B9762AMG provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 4095) while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA} = (\text{DAC CODE}/4096) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (4095 - \text{DAC CODE})/4096 \times I_{OUTFS} \quad (2)$$

where DAC CODE = 0 to 4095 (i.e., Decimal Representation). As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

$$\text{where } I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, which are tied to analog common, GND_A. Note, R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50Ω or 75Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply :

$$VOUTA = IOUTA \times RLOAD \quad (5)$$

$$VOUTB = IOUTB \times RLOAD \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance. The differential voltage, V_{DIFF}, appearing across I_{OUTA} and I_{OUTB} is:

$$VDIFF = (IOUTA - IOUTB) \times RLOAD \quad (7)$$

Substituting the values of IOUTA, IOUTB, and IREF; VDIFF can be expressed as:

$$VDIFF = \{(2\ DAC\ CODE - 4095)/4096\} \times (32\ RLOAD/RSET) \times VREFIO \quad (8)$$

These last two equations highlight some of the advantages of operating the B9762AMG differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB})

or differential output (V_{DIFF}) of the B9762AMG can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

7.1.2 Reference Operation

The B9762AMG contains an internal 1.20V bandgap reference that can be easily disabled and overridden by an external reference. REFIO serves as either an input or output depending on whether the internal or an external reference is selected. If REFLO is tied to GNDA, as shown in Figure 7-2, the internal reference is activated and REFIO provides a 1.20V output. In this case, the internal reference must be compensated externally with a ceramic chip capacitor of 0.1 µF or greater from REFIO to REFLO. Also, REFIO should be buffered with an external amplifier having an input bias current less than 100 nA if any additional loading is required.

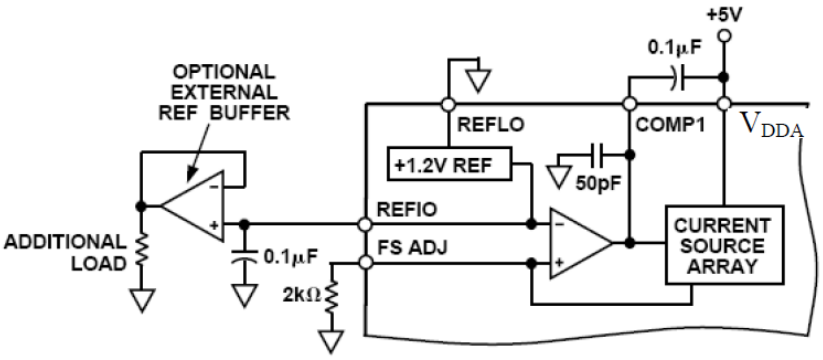


Figure 7-2. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to V_{DDA}. In this case, an external reference may then be applied to REFIO as shown in Figure 7-3. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1 MΩ) of REFIO minimizes any loading of the external reference.

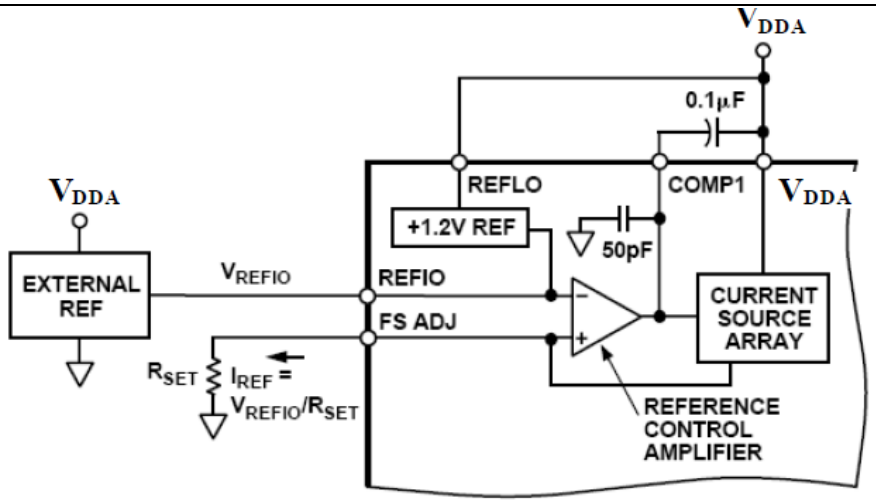


Figure 7-3. External Reference Configuration

7.1.3 Reference Control Amplifier

The B9762AMG also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter as shown in Figure 7-3, such that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied over to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide adjustment span of I_{OUTFS} over a 2mA to 20mA range by setting I_{REF} between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the B9762AMG, which is proportional to I_{OUTFS} (refer to the POWER DISSIPATION section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier can be reduced by connecting an external capacitor between COMP1 and V_{DDA}. The output of the control amplifier, COMP1, is internally compensated via a 50 pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Any additional external capacitance further limits the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier.

The optimum distortion performance for any reconstructed waveform is obtained with a 0.1 µF external capacitor installed. Thus, if I_{REF} is fixed for an application, a 0.1 µF ceramic chip capacitor is recommended. Also, since the control amplifier is optimized for low power operation, multiplying applications requiring large signal swings should consider using an external control amplifier to enhance the

application's overall large signal multiplying bandwidth and/or distortion performance.

There are two methods in which I_{REF} can be varied for a fixed R_{SET}. The first method is suitable for a single-supply system in which the internal reference is disabled, and the common-mode voltage of REFIO is varied over its compliance range of 1.25V to 0.10V. REFIO can be driven by a single-supply amplifier or DAC, thus allowing I_{REF} to be varied for a fixed RSET. A simple, low cost R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 7-4 using the AD7524 and an external 1.2 V reference, the AD1580.

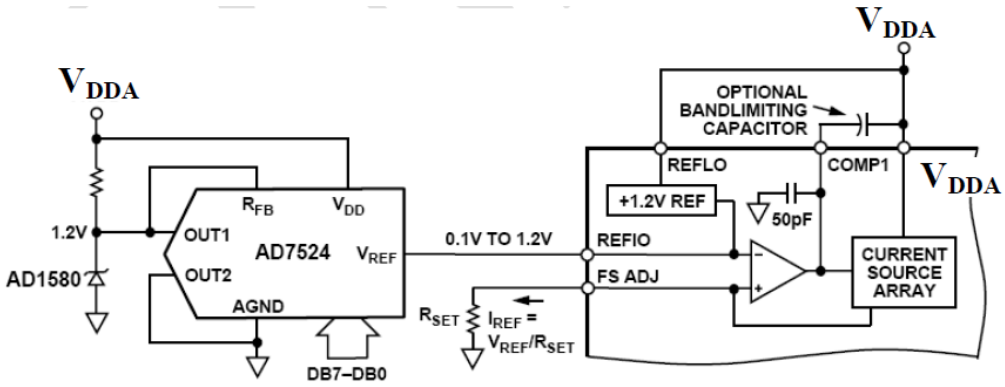


Figure 7-4. Single-Supply Gain Control Circuit

The second method may be used in a dual-supply system in which the common-mode voltage of REFIO is fixed and I_{REF} is varied by an external voltage, V_{GC}, applied to R_{SET} via an amplifier. An example of this method is shown in Figure 7-5 in which the internal reference is used to set the common-mode voltage of the control amplifier to 1.20V. The external voltage, V_{GC}, is referenced to GND_A and should not exceed 1.2V. The value of R_{SET} is such that I_{REFMAX} and I_{REFMIN} do not exceed 62.5μA and 625μA, respectively. The associated equations in Figure 7-5 can be used to determine the value of R_{SET}.

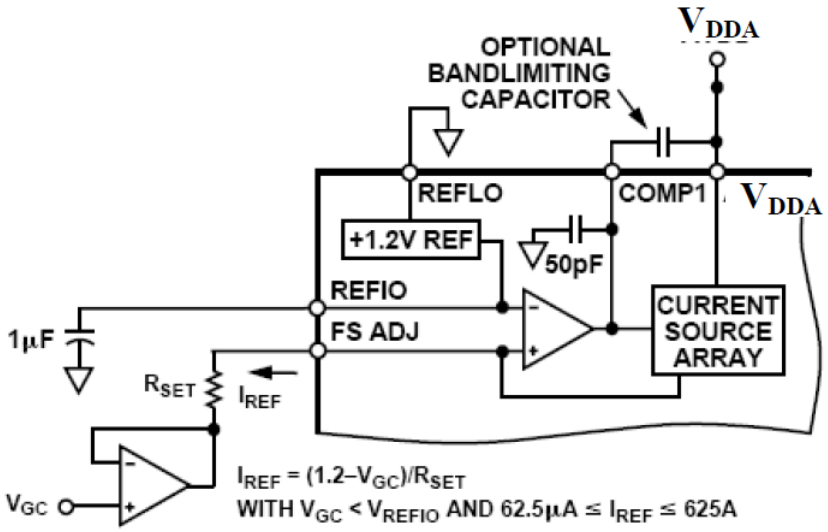


Figure 7-5. Dual-Supply Gain Control Circuit

In some applications, the user may elect to use an external control amplifier to enhance the multiplying bandwidth, distortion performance, and/or settling time. External amplifiers capable of driving a 50pF load such as the AD817 are suitable for this purpose. It is configured in such a way that it is in parallel with the weaker internal reference amplifier as shown in Figure 7-6. In this case, the external amplifier simply overdrives the weaker reference control amplifier. Also, since the internal control amplifier has a limited current output, it will sustain no damage if overdriven.

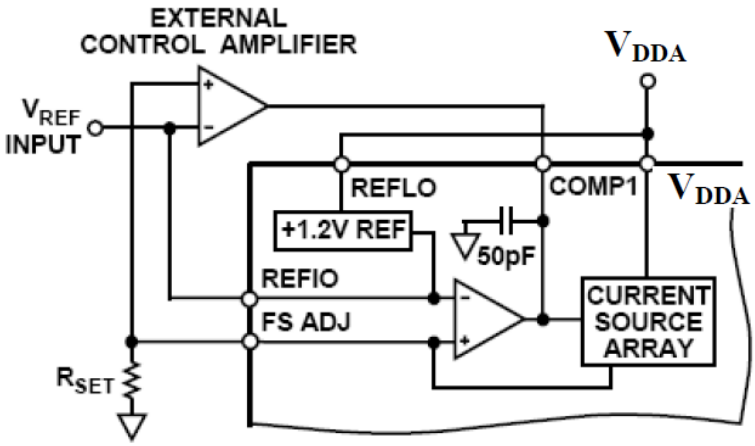


Figure 7-6. Configuring an External Reference Control Amplifier

7.1.4 Analog Outputs

The B9762AMG produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC TRANSFER FUNCTION section

by equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the B9762AMG is optimum and specified using a differential transformer coupled output in which the voltage swing at I_{OUTA} and I_{OUTB} is limited to ±0.5 V. If a single-ended unipolar output is desirable, I_{OUTA} should be selected.

The distortion and noise performance of the B9762AMG can be enhanced when the B9762AMG is configured for differential operation. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (i.e., assuming no source termination). Since the output currents of I_{OUTA} and I_{OUTB} are complementary, they become additive when processed differentially. A properly selected transform- er will allow the B9762AMG to provide the required power and voltage levels to different loads.

The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100kΩ in parallel with 5pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground via an I-V op amp configuration will result in the optimum dc linearity.

7.1.5 Digital Inputs

The B9762AMG's digital input consists of 12 data input pins and a clock input pin. The 12-bit parallel data inputs follow standard positive binary coding where DB11 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch.

The DAC output is updated following the rising edge of the clock and is designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse width. The set-up and hold times can also be varied within the clock cycle as long as the specified minimum times are met; although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

The internal digital circuitry of the B9762AMG is capable of operating over a digital supply range of 3.3V to 5V. Figure 7-7 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar with the exception that it contains an active pull-down circuit, thus ensuring that the B9762AMG remains enabled if this input is left disconnected.

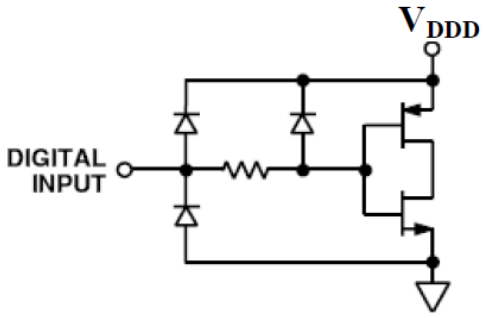


Figure 7-7. Equivalent Digital Input

Since the B9762AMG is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum set-up and hold times of the B9762AMG as well as its required min/max input logic level thresholds. Typically, the selection of the slowest logic family that satisfies the above conditions will result in the lowest data feedthrough and noise.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20Ω to 100Ω) between the B9762AMG digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain “clean” digital inputs.

The external clock driver circuitry should provide the B9762AMG with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a

reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

7.1.6 Sleep Mode Operation

The B9762AMG has a powerdown function which turns off the output current and reduces the supply current . This mode can be activated by applying a logic level "1" to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures the B9762AMG remains enabled if this input is left disconnected.

7.1.7 Power Dissipation

The power dissipation, PD, of the B9762AMG is dependent on several factors which include:

(1) V_{DDA} and V_{DDD}, the power supply voltages;

(2) I_{OUTFS}, the full-scale current output;

(3) f_{CLOCK}, the update rate;

(4) the reconstructed digital input waveform.

7.2 Applications

7.2.1 Output Configurations

The following sections illustrate some typical output configurations for the B9762AMG. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD}, referred to GND_A. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note, I_{OUTA} provides slightly better performance than I_{OUTB}.

7.2.2 Differential Coupling Using A Transformer

An RF transformer can be used to perform a differential-to single-ended signal conversion as shown in Figure 7-8. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

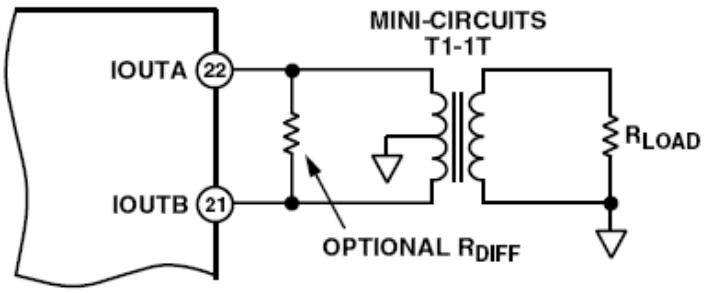


Figure 7-8. Differential Output Using a Transformer

Differential Output Using a Transformer The center tap on the primary side of the transformer must be connected to GND_A to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around GND_A and should be maintained with the specified output compliance range of the B9762AMG. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

7.2.3 Differential Using An Op Amp

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 7-9. The B9762AMG is configured with two equal load resistors, R_{LOAD}, of 25Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted

to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB} forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

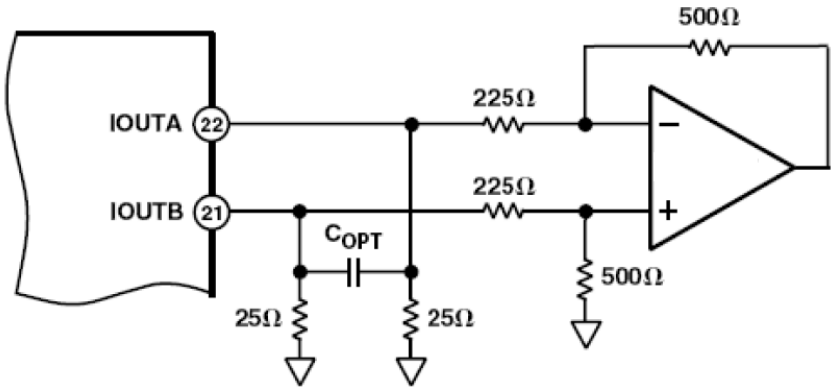


Figure 7-9. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ±1.0V.

The differential circuit shown in Figure 7-10 provides the necessary level-shifting required in a single supply system. In this case, V_{DDA} which is the positive analog supply for both the B9762AMG and the op amp is also used to level-shift the differential output of the B9762AMG to midsupply (i.e., $V_{DDA}/2$).

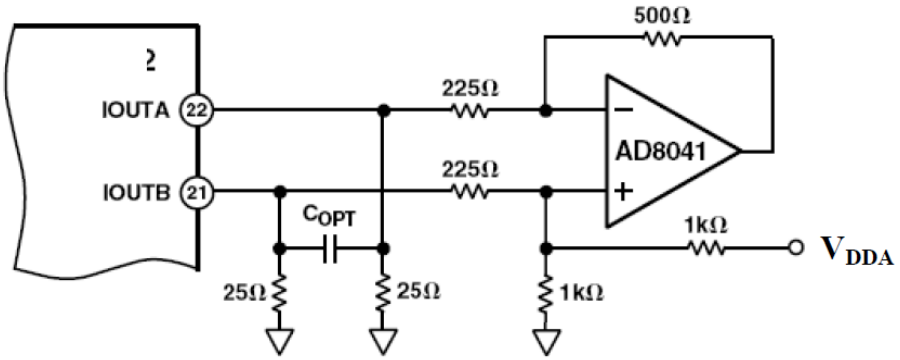


Figure 7-10. Single-Supply DC Differential Coupled Circuit

7.2.4 Single-Ended Unbuffered Voltage Output

Figure 7-11 shows the B9762AMG configured to provide a unipolar output range of approximately 0V to +0.5V for a doubly terminated 50Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB}. The

unused output (I_{OUTA} or I_{OUTB}) can be connected to GND_A directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

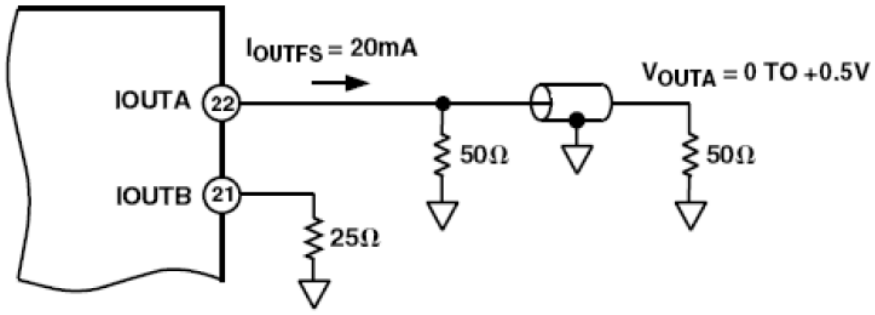


Figure 7-11. 0 V to +0.5 V Unbuffered Voltage Output

7.2.5 Single-Ended, Buffered Voltage Output Configuration

Figure 7-12 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the B9762AMG output current. U1 maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the ANALOG OUTPUT section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of RFB and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or RFB. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

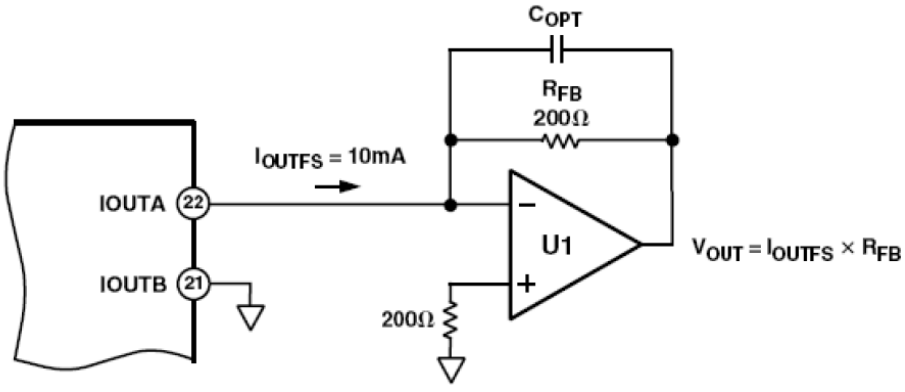


Figure 7-12. Unipolar Buffered Voltage Output

7.2.6 Power And Grounding Considerations

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection; placement and routing; and supply bypassing and grounding.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The B9762AMG features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, V_{DDA}, the analog supply, should be decoupled to GND_A, the analog common, as close to the chip as physically possible. Similarly, V_{DDD}, the digital supply, should be decoupled to GND_D as close as physically as possible.

For those applications that require a single +5V or +3.3V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 7-13. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

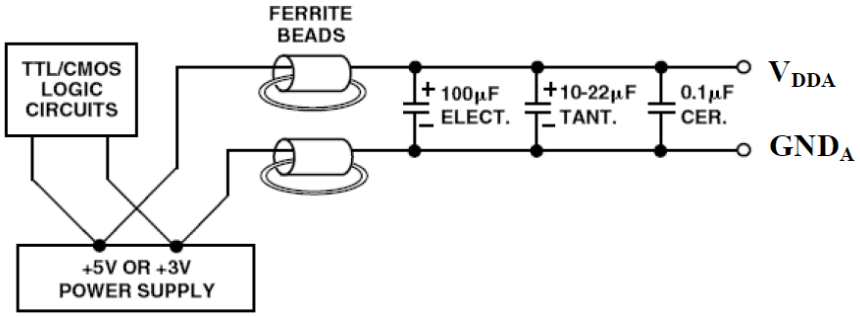


Figure 7-13. Differential LC Filter for Single +5V or +3.3V Applications

7.3 Absolute Maximum Ratings

1) Power Voltage(V_{DDD},V_{DDA})……-0.3V ~ 6.5 V
2) Digital Input Voltage(V_{ID})……...-0.3V ~ V_{DDD}+0.3V
3) Digital Input&Output Voltage (V_{IA},V_{OA})……-0.3V ~ V_{DDA}+0.3V
4) Reference Voltage(V_{IREF})……0.1V ~ 1.35V
5) IOUTA,IOUTB Output Voltage(V_{IOIUTA},V_{IOUTB})……....-1.0V ~ 1.25V
6) Storage Temperature(TSTG)……-65℃ ~ + 150℃
7) Lead Temperature (10 sec)(T_h)……..260℃
8) Junction Temperature(T_J)……150℃
9) Thermal Resistance($R_{th(jc)}$) ……20℃/W

7.4 Recommended Operating Conditions

1) Power Voltage(V_{DDD},V_{DDA})……3.15V ~ 5.25 V

2) Output Resistance……50Ω

3) Temperature Range(T_A)……..-55℃ ~ 125℃

7.5 Storage Condition

The warehouse environment of B9762AMG should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

Table 7-1. The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

7.6 Radiation hardened performance

a) Total Ionizing Dose ≥ 100 Krad(Si)

8. Electrical Specification

V_{DDD}=V_{DDA}=5V， -55℃≤T_A≤125℃, I_O = 20mA, unless otherwise specified.

Table 8-1. Electronic Specifications

Parameter	symbol	Condition（V_{DDD}=V_{DDA}=5V ） Io=20mA -55℃ ≤ T_A ≤ 125℃	Value		Unit
			min	Max	
INL	E_L		-4.5	+4.5	LSB
DNL	E_{DL}		-2.5	+2.5	LSB
Offset Error	E_O		-0.1	+0.1	%FS
Gain Error	E_G		-10.0	+10.0	%FS
Reference Output Voltage	V_{REF}		1.08	1.32	V

Parameter	symbol	Condition (V_{DDD}=V_{DDA}=5V ） Io=20mA -55℃ ≤ T_A ≤ 125℃	Value		Unit
			min	Max	
CMOS INPUTS Logic 1 Voltage	V_{IH}	V_{DDD}= 5V	3.5	—	V
CMOS INPUTS Logic 1 Voltage	V_{IH}	V_{DDD}= 3.3V	2.4	—	V
CMOS INPUTS Logic 0 Voltage	V_{IL}	V_{DDD}= 5V	—	1.3	V
CMOS INPUTS Logic 0 Voltage	V_{IL}	V_{DDD}= 3.3V	—	0.8	V
Input Current	I_{IH}	V_I=5V	-10.0	10.0	μA
Input Current	I_{IL}	V_I=0V	-10.0	10.0	μA
Offset Drift (TEMPERATURE)	α_{EO}		-0.02	+0.02	%FS/℃
Gain Drift (TEMPERATURE)	α_{EG}		-0.1	+0.1	%FS/℃
Reference Voltage Drift (TEMPERATURE)	α_{VREF}		-0.0002	+0.0002	1/℃
Analog Supply Current	I_{DDA}	50Ω	—	35.0	mA
Digital Supply Current	I_{DDD}	50Ω，fCLK=25MSPS fO=1.0MSPS	—	3.0	mA
Power Dissipation	P_W	50Ω， fCLK =25MSPS fO =1.0MSPS	—	220	mW
SPURIOUS-FREE DYNAMIC RANGE	*SFDR*	f_{CLK} =25MHz，f_O =1MHz,	66.0	—	dBc
		f_{CLK} =50MHz， f_O,=1MHz,	66.0	—	dBc
		f_{CLK} =50MHz， f_O =2MHz,	60.0	—	dBc
		f_{CLK} =60MHz， f_O =1MHz,	66.0	—	dBc
		f_{CLK} =100MHz， f_O =1MHz,	65.0	—	dBc
		f_{CLK} =120MHz， f_O =1MHz,	63.0	—	dBc
TOTAL	*THD*	f_{CLK} =25MHz， f_O =1MHz,	—	-66.0	dBc

Parameter	symbol	Condition (V_{DDD}=V_{DDA}=5V ） Io=20mA -55℃ ≤ T_A ≤ 125℃	Value		Unit
			min	Max	
HARMONIC DISTORTION		f_{CLK} =50MHz， f_O =1MHz,	—	-66.0	dBc
		f_{CLK} =50MHz， f_O =2MHz,	—	-58.0	dBc
		f_{CLK} =60MHz， f_O =1MHz,	—	-66.0	dBc
		f_{CLK} =100MHz， f_O =1MHz,	—	-64.0	dBc
		f_{CLK} =120MHz， f_O =1MHz,	—	-62.0	dBc
Output Setup Time	t_{su}		—	50.0	ns
Maximum Frequency	f_{max}		100.0	—	MHz

9. Typical Application（Appendix 2）

10. Outline Dimensions

CPGA28 Packaging.

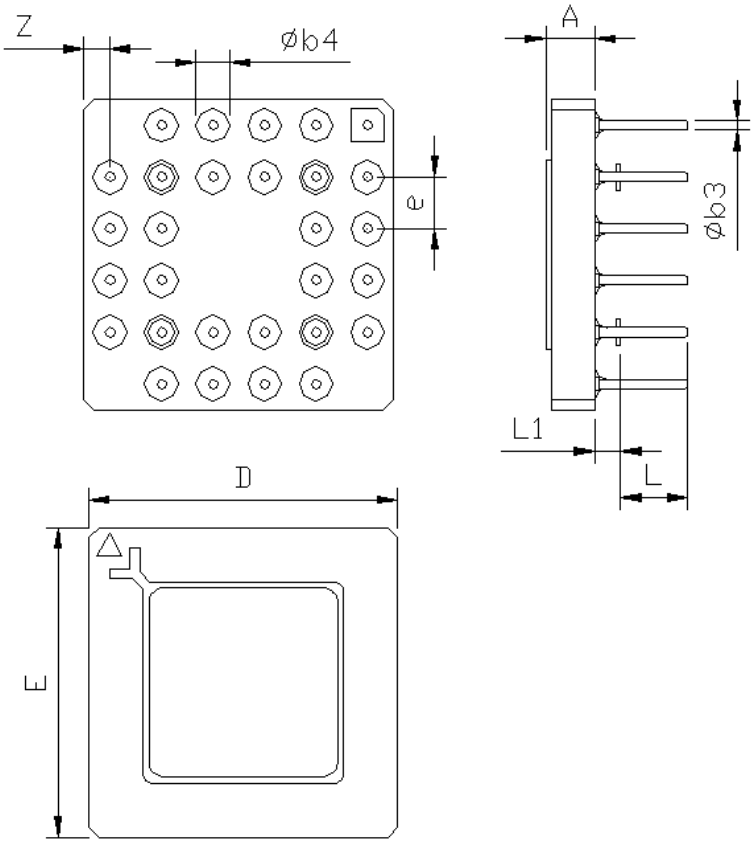


Figure 10-1. B9762AMG's Packaging(CPGA28)

Symbol	Values(Units:mm)		
	Min.	Typ.	Max.
D	15.09	——	15.39
E	15.09	——	15.39
Z	——	1.27	——
A	1.78	——	3.68
e	——	2.54	——
L1	1.02	——	1.52
L	2.54	——	5.08
Φb3	0.41	——	0.51
Φb4	1.50	——	1.80

Appendix 1. Pin Definition

Appendix Table1-1 Pin Definition

Pin	Symbol	type	Property	Pin	Symbol	type	Property
A3	D11	I	Most Significant Data Bit (MSB)	F4	SLEEP	I	Power-Down Control Input。HI：Sleep。LO：normal
B3	D10	I	Data Bit 10	E4	REFLO	I	Reference choose. 1) Connect to VDDA to disable internal reference . 2)Ground when Internal 1.2 V Reference Used.
A2	D 9	I	Data Bit 9	F5	V_{REF}	I /O	Reference Input/Output
B2	D8	I	Data Bit 8	E5	FSADJ	I	Full-Scale Current Output Adjust
B1	D7	I	Data Bit 7	E6	COMP1	I	Bandwidth/Noise Reduction Node. Add 0.1 μF to VDDA for optimum performance.
C2	D6	I	Data Bit 6	D5	GND_A	G	Analog Common.
C1	D5	I	Data Bit 5	D6	IOUTB	O	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
D1	D4	I	Data Bit 4	C6	IOUTA	O	DAC Current Output. Full-scale current when all data bits are 1s.
D2	D3	I	Data Bit 3	C5	COMP2	O	Internal Bias Node for Switch Driver Circuitry. Decouple to GND with 0.1 μF capacitor
E1	D2	I	Data Bit 2	B6	V_{DDA}	P	Analog Supply Voltage
E2	D1	I	Data Bit 1	B5	NC	NC	No connect

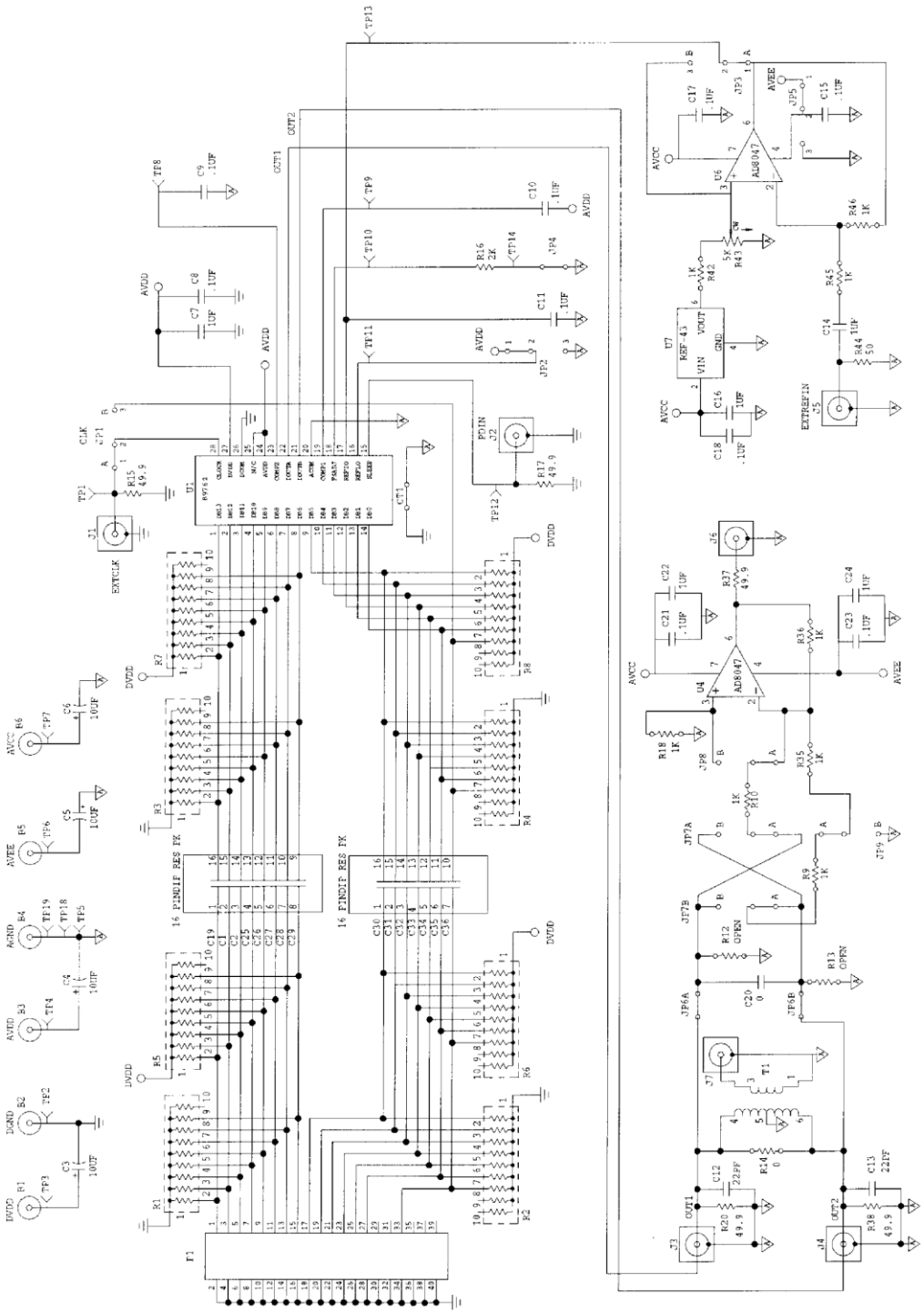
F2	D0	I	Least Significant Data Bit (LSB)	A5	GND_D	G	Digital Common.
E3	NC	I	No Contact	B4	V_{DDD}	P	Digital Supply Voltage (+3.3 V or +5 V).
F3	NC	I	No Contact	A4	CLK	I	Clock Input. Data latched on positive edge of clock
A1	NC		No Contact				

Appendix 2. Typical Applications

Applications

Communication Transmit Channel, Basestations, ADSL/HFC Modems

Evaluation Board



Appendix 2-1. Evaluation Board Schematic

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